

LCFC Confidential

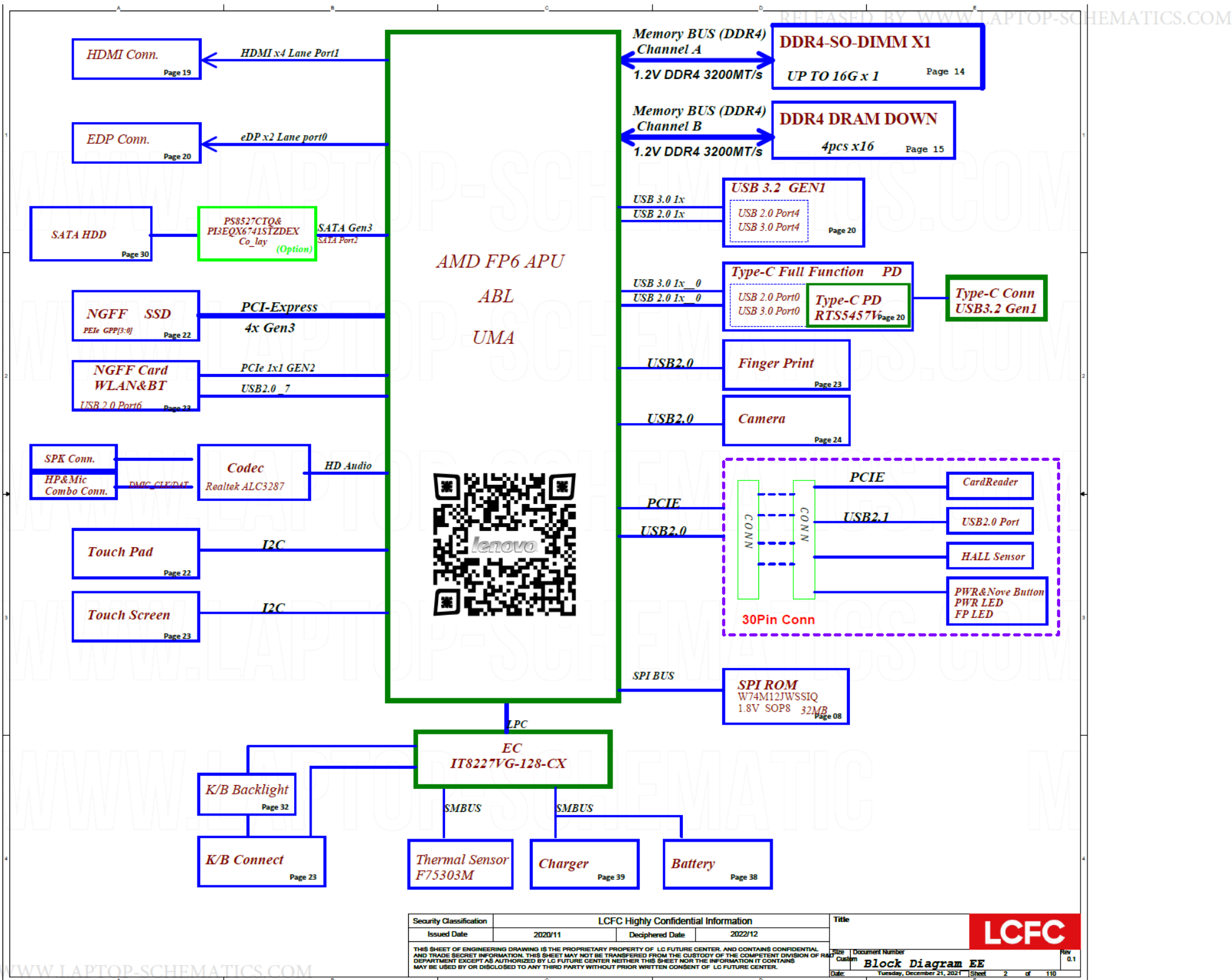
JS471/JS573 NM-E541 Schematics Document

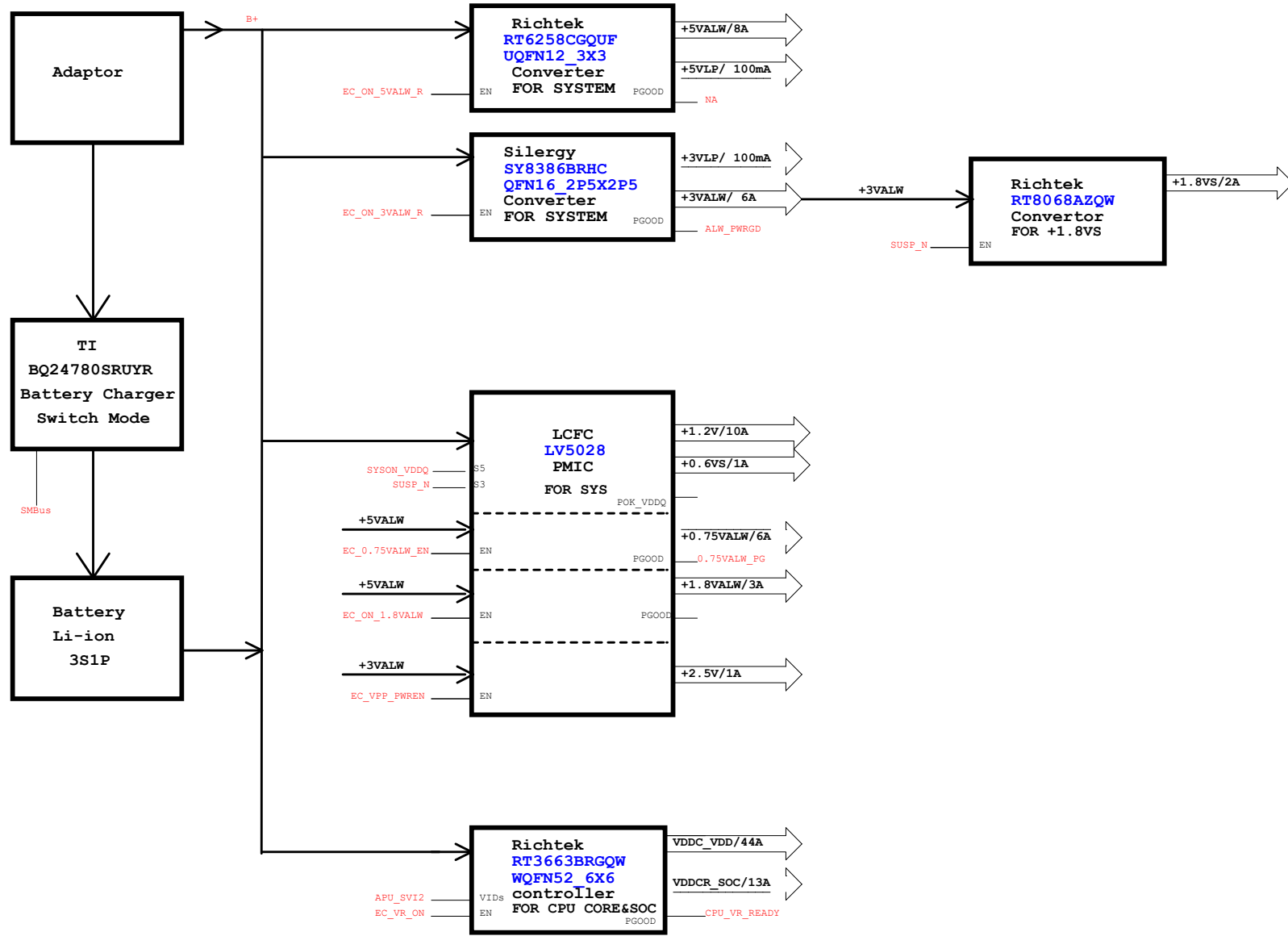
AMD FP6 ABL with DDR4

2021-04-28

REV: 0.1

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Issued Date	2020/11	Deciphered Date	2022/12			
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane State	B+ +3VL +5VL	+3VALW +5VALW +1.8VALW +0.75VALW		+1.2V +2.5V_DDR	+5VS +3VS +1.8VS +0.75VS +0.6VS +VDDC_VDD +VDDCR_SOC	
S0	O	O		O	O	O
S0Ix						
S3	O	O		O	X	X
S3 Battery only	O	O		O	X	X
S5 S4 AC Only	O	O		X	X	X
S5 S4 Battery only	O	X		X	X	X
S5 S4 AC & Battery don't exist	X	X		X	X	X

HSIO Matrix

HSIO PORT	Function
USB2.0	0 Type-C USB2.0 Port 0
	1 USB3.0_P1
	2 Camera
	3 Touch Screen Change to I2C
	4 USB2.0 Port(For DB USB2.0)
	5
	6 FingerPrint
	7 BT
USB3.0	0 Type-C USB3.0 Port 0
	1 USB3.0_P1
	4 NC
	5 NC
DisPlay	0 eDP 2*Lane
	1 HDMI
	2 NC
	3 NC
PCIE/ SATA	PCIE0 LAN&Cardreader
	PCIE1 WLAN
	PCIE2/SATA0 SATA HDD
	PCIE3/SATA1 N/A
	PCIE4 N/A
	PCIE5 N/A
	PCIE6 N/A
	PCIE7 N/A
	PCIE8/SATA2
	PCIE9/SATA3 SSD
	PCIE10
	PCIE11

SMBUS Control Table OK

Source Slave	EC IT8227C				PCH			
	EC_SMB_0 +3VS	EC_SMB_1 +3VL_EC	EC_SMB_3 +3VL_EC	EC_SMB_2 +3VL_EC	I2C0 1.8VS/3.3VS	I2C1 1.8VS/3.3VS	I2C2/SMBUS 1.8VS/3.3VS	USBC_I2C_SDA/CLK +1.8VALW
DGPU								
Memory Down	X	X	X	X	X	X	X	X
SODIMM							V 3VS	
BATT	X	V +3VL_EC	X	X	X	X	X	X
Charger	X	V +3VL_EC	X	X	X	X	X	X
WLAN	X	X	X	X	X	X	X	X
PMIC	X	X	V +3VL_EC	X	X	X	X	X
	X	X	X	X	X	X	X	X
Thermal Sensor	V +3VS	X	X	X	X	X	X	X
LPC&TS	X	X	X	X	V +3VS_CPU	X	X	X
TP	X	X	X	X	X	V 3VS	X	X
PD	X	X	X	V +3VL	X	X	X	V +1.8VALW
	X	X	X	X	X	X	X	X

EC SMBus0 address

Device	Address
DGPU	
Thermal Sensor(NCT7718W)	
Thermal Sensor(NCT7719W)	1001_101xb
TOF	

EC SMBus1 address

Device	Address
Smart Battery	0x16
Charger	0x12

EC SMBus3 address

Device	Address
IMVP9	
PMIC	0x34

EC SMBus4 address

Device	Address
PD	TBD

PCH SML0 address

Device	Address
Re-Timer	TBD

PCH SML1 address

Device	Address
PD	TBD

PCH ISH I2C0 address

Device	Address
TOF	
Accelerometer(MB)	001 1000b
Accelerometer(DB)	001 1001b
Light Sensor	1000 100xb



D

C

B


A

D

C


B

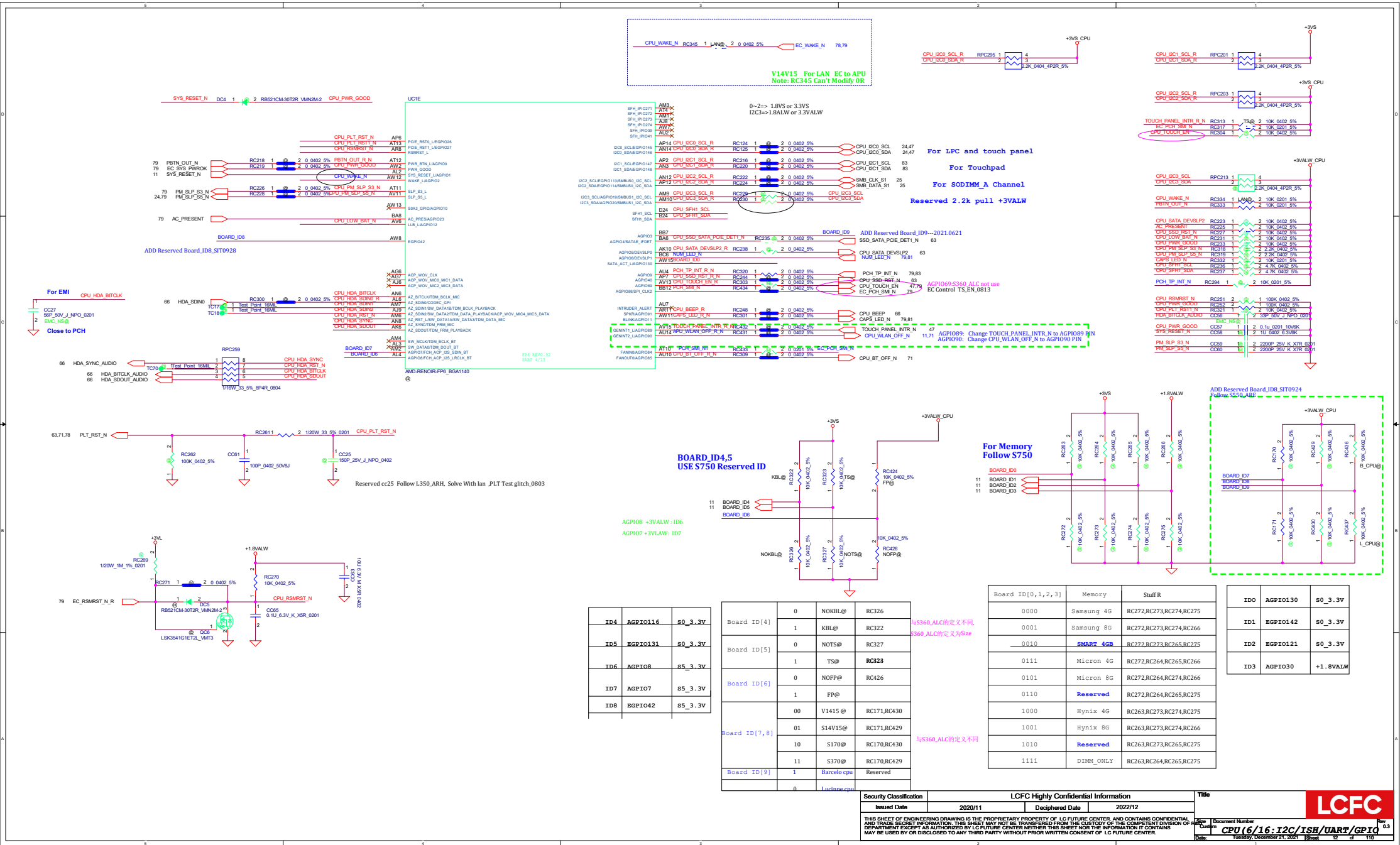
A

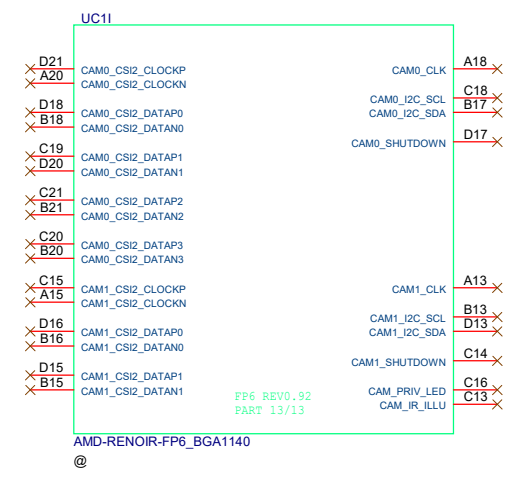
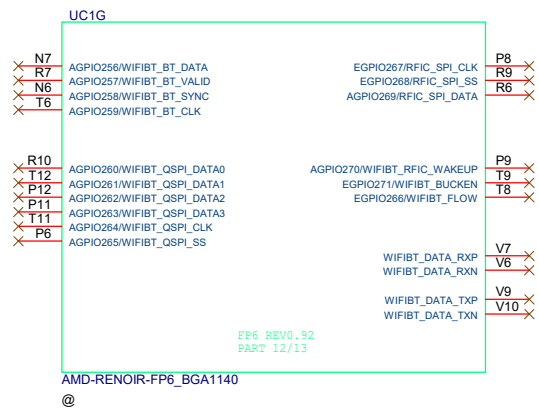
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PD FW Update

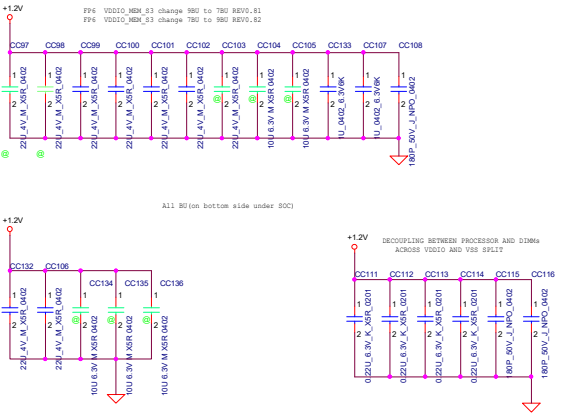
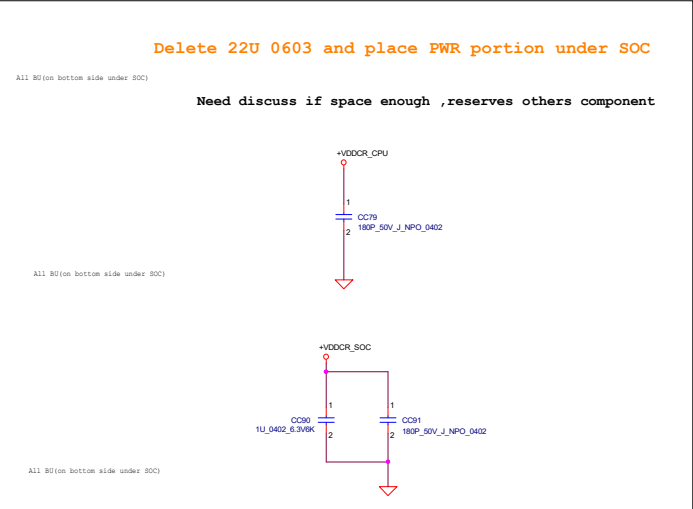
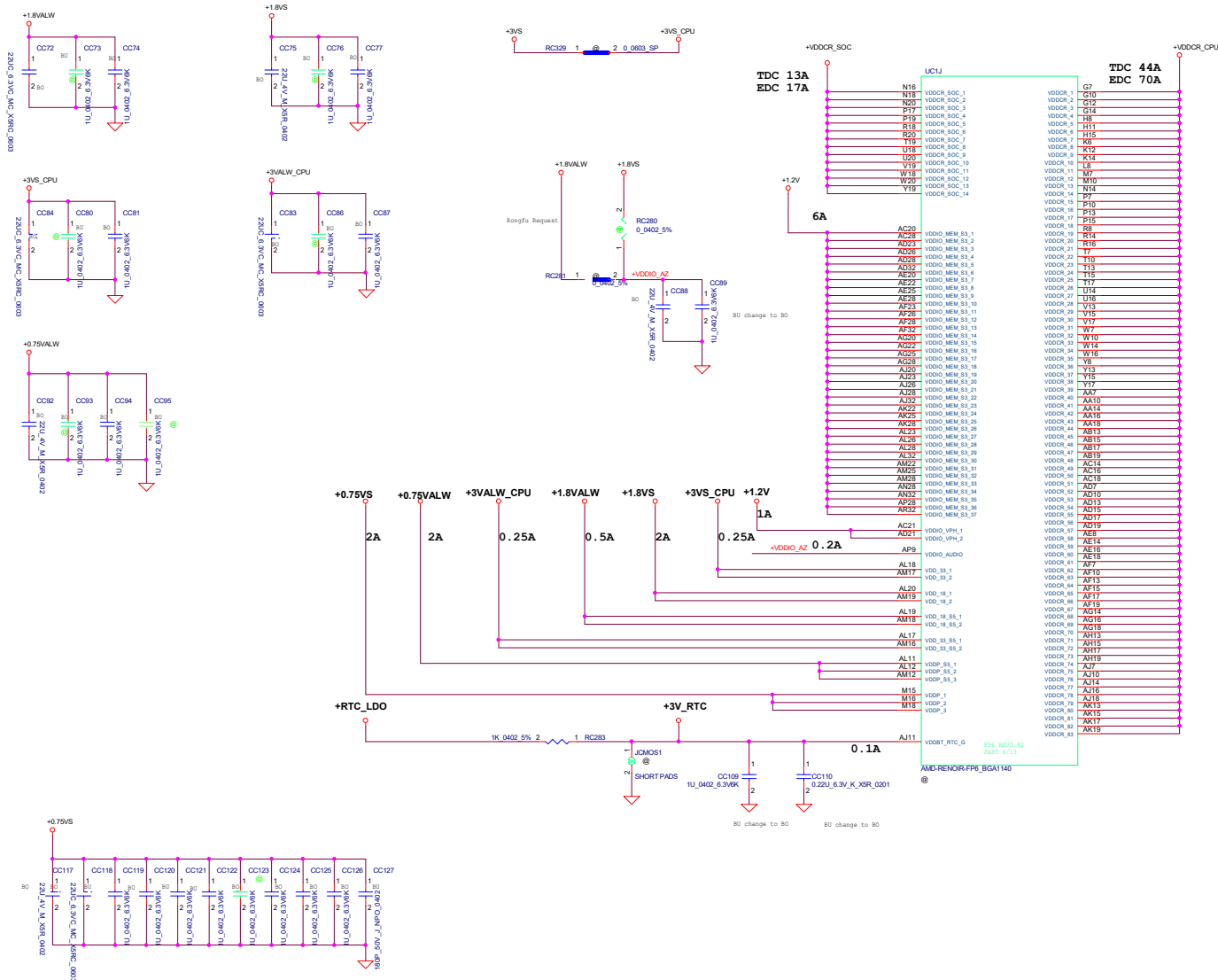
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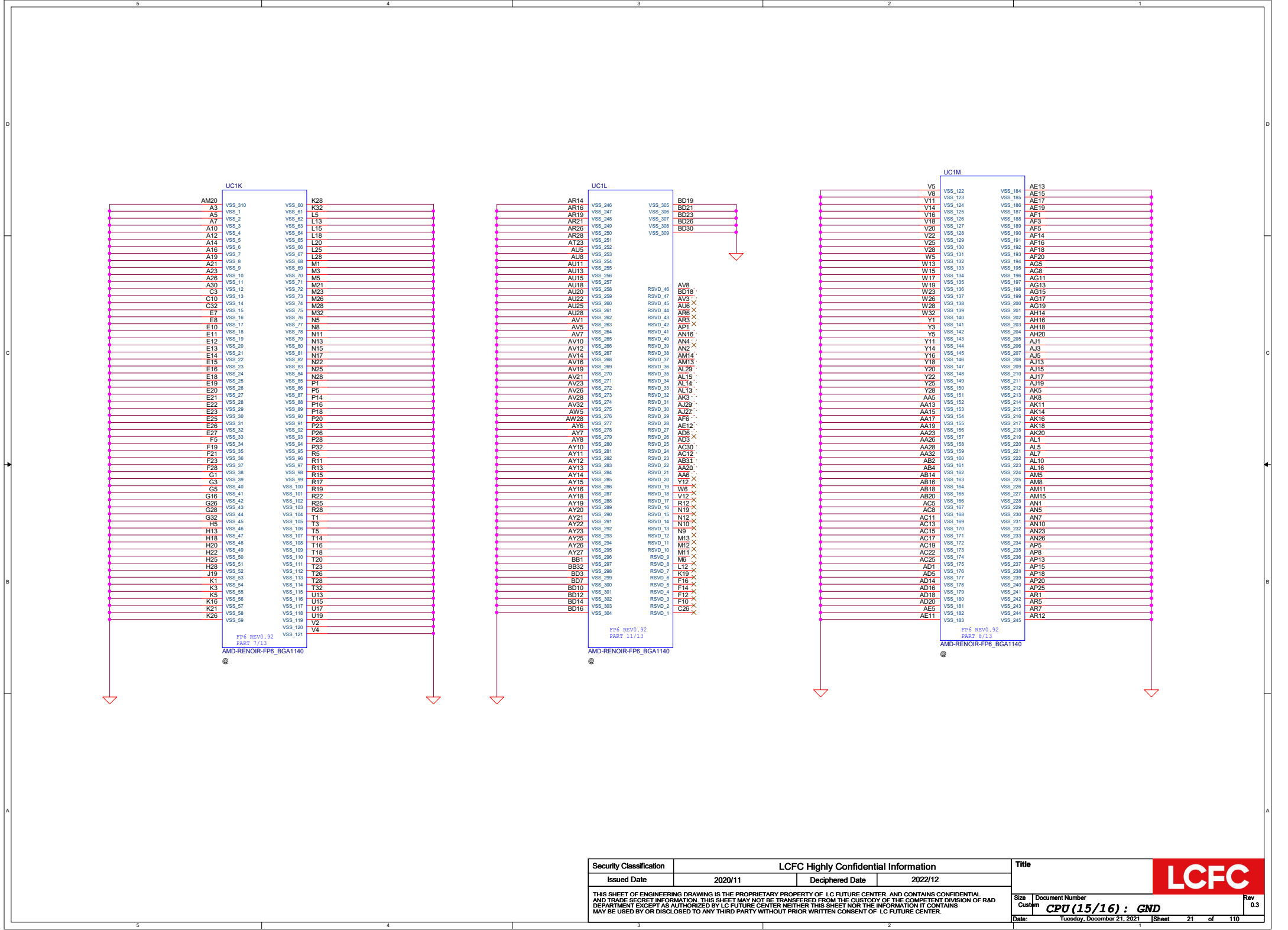
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				Custom	0.3
				CPU(15/16) : GND	
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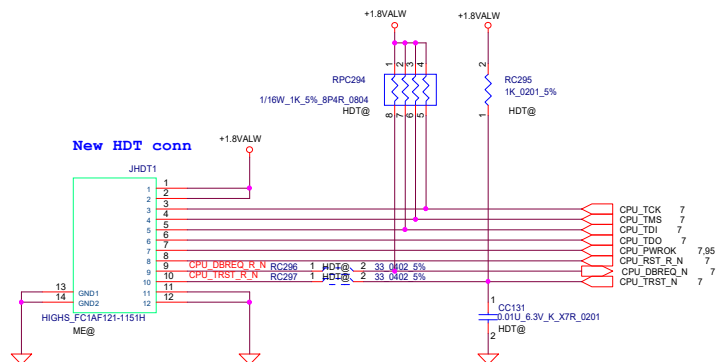


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C	PCH PWR Reserved	Rev	0.3
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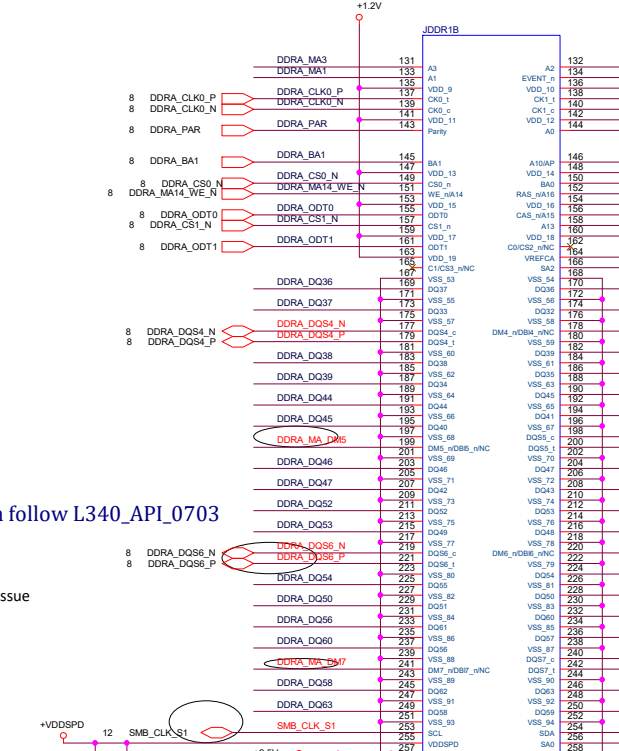
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D																								
C																								
B																								
A																								
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HDT Debug Header



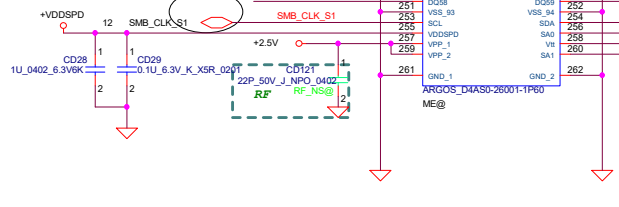
Title		LCFC
Size C	Document Number XDP	
Date: <u>September 21, 2009</u> (Sheet <u>24</u> of <u>44</u>)		Rev 0.3

DDRA_DQ[0..63]	< >	DDRA_DQ[0..63]	8
DDRA_MA[0..13]	◁ ▷	DDRA_MA[0..13]	8
DDRA_MA_DM[0..7]	◁ ▷	DDRA_MA_DM[0..7]	8

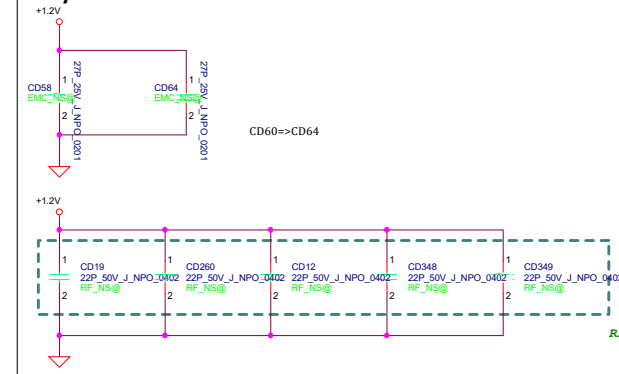


Pin Name	Net Name
DQ0	DRA_DQ0
DQ1	DRA_DQ5
DQ2	DRA_DQ2
DQ3	DRA_DQ3
DQ4	DRA_DQ4
DQ5	DRA_DQ0
DQ6	DRA_DQ1
DQ7	DRA_DQ7
DQS#0	DRA_DQS#0
DQS0	DRA_DQS0
DQ8	DRA_DQ13
DQ9	DRA_DQ9
DQ10	DRA_DQ14
DQ11	DRA_DQ10
DQ12	DRA_DQ7
DQ13	DRA_DQ8
DQ14	DRA_DQ15
DQ15	DRA_DQ11
DQS#1	DRA_DQS#1
DQS1	DRA_DQS1
DQ16	DRA_DQ20
DQ17	DRA_DQ21
DQ18	DRA_DQ22
DQ19	DRA_DQ19
DQ20	DRA_DQ16
DQ21	DRA_DQ17
DQ22	DRA_DQ23
DQ23	DRA_DQ18
DQS#2	DRA_DQS#2
DQS2	DRA_DQS2
DQ24	DRA_DQ28
DQ25	DRA_DQ29
DQ26	DRA_DQ31
DQ27	DRA_DQ27
DQ28	DRA_DQ24
DQ29	DRA_DQ25
DQ30	DRA_DQ30
DQ31	DRA_DQ26
DQS#3	DRA_DQS#3
DQS3	DRA_DQS3
DQ32	DRA_DQ33
DQ33	DRA_DQ37
DQ34	DRA_DQ34
DQ35	DRA_DQ38
DQ36	DRA_DQ32
DQ37	DRA_DQ36
DQ38	DRA_DQ35
DQ39	DRA_DQ39
DQS#4	DRA_DQS#4
DQS4	DRA_DQS4
DQ40	DRA_DQ44
DQ41	DRA_DQ40
DQ42	DRA_DQ47
DQ43	DRA_DQ43
DQ44	DRA_DQ41
DQ45	DRA_DQ45
DQ46	DRA_DQ46
DQ47	DRA_DQ42
DQS#5	DRA_DQS#5
DQS5	DRA_DQS5
DQ48	DRA_DQ48
DQ49	DRA_DQ49
DQ50	DRA_DQ50
DQ51	DRA_DQ50
DQ52	DRA_DQ52
DQ53	DRA_DQ53
DQ54	DRA_DQ54
DQ55	DRA_DQ55
DQS#6	DRA_DQS#6
DQS6	DRA_DQS6
DQ56	DRA_DQ60
DQ57	DRA_DQ56
DQ58	DRA_DQ63
DQ59	DRA_DQ59
DQ60	DRA_DQ61
DQ61	DRA_DQ57
DQ62	DRA_DQ58
DQ63	DRA_DQ62
DQS#7	DRA_DQS#7
DQS7	DRA_DQS7

for MEM_MB_RST# overshoot issue



Layout Note: Place near JDDR1

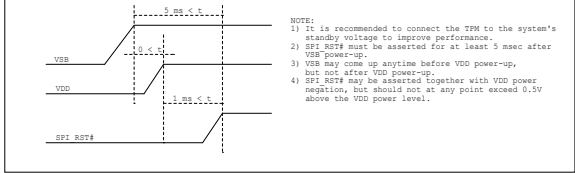


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Title		LCFC	
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Custom	DDRIV SO-DIMM A	0.1	
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TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS20
ST Micro	ST33HTPH2E32AHC0	SA000089E20

NOTE:
Check timing sequence in SDV phase.

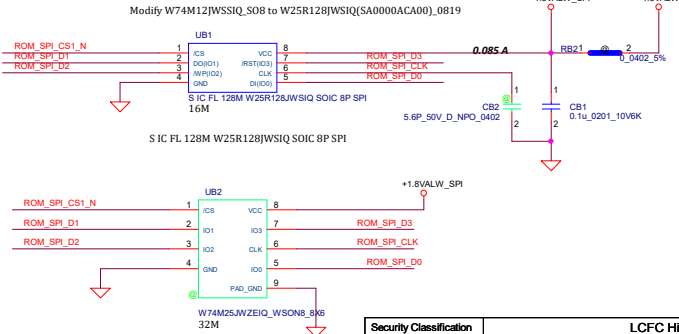
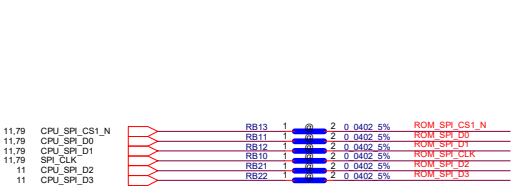


- NOTE:
- 1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
 - 2) SPI_RST# must be asserted for at least 5 msec after VSB power-up.
 - 3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
 - 4) SPI_RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

TABLE			
Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

SPI ROM

Used RPMC BIOS ROM



Need to confirm with BIOS 32M or 16M7_0428

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				Date	110

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C	GPU PCIE Interface	0.3	
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C	GPU STRAP/DP/HDMI	Rev	0.3
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C	GPU MEM Interface	Rev	0.3
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Title			
Size	Document Number		
C	GPU Strap	Date:	Rev
Tuesday, December 21, 2021		Sheet	110



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Title			
Size	Document Number		
C	GPU PWR1	Rev	0.3
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Title

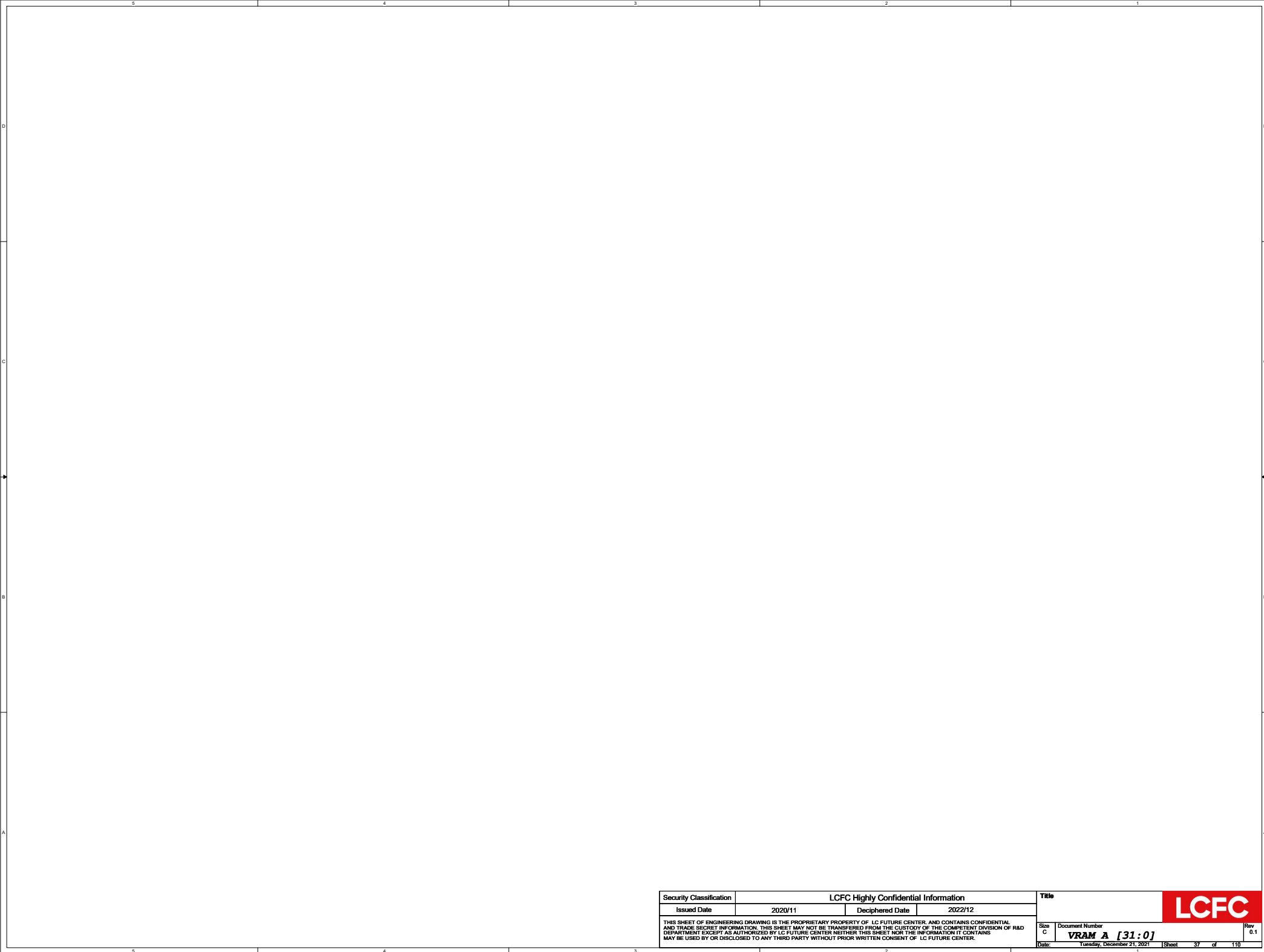
LCFC

Size	Document Number	Rev
C	GPU_PWR2	0.3
Date:	Tuesday, December 21, 2021	Sheet 35 of 110




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Title			
Size	Document Number		
C	GPU GND	Rev	0.3
Date:	Tuesday, December 21, 2021	Sheet	36 of 110




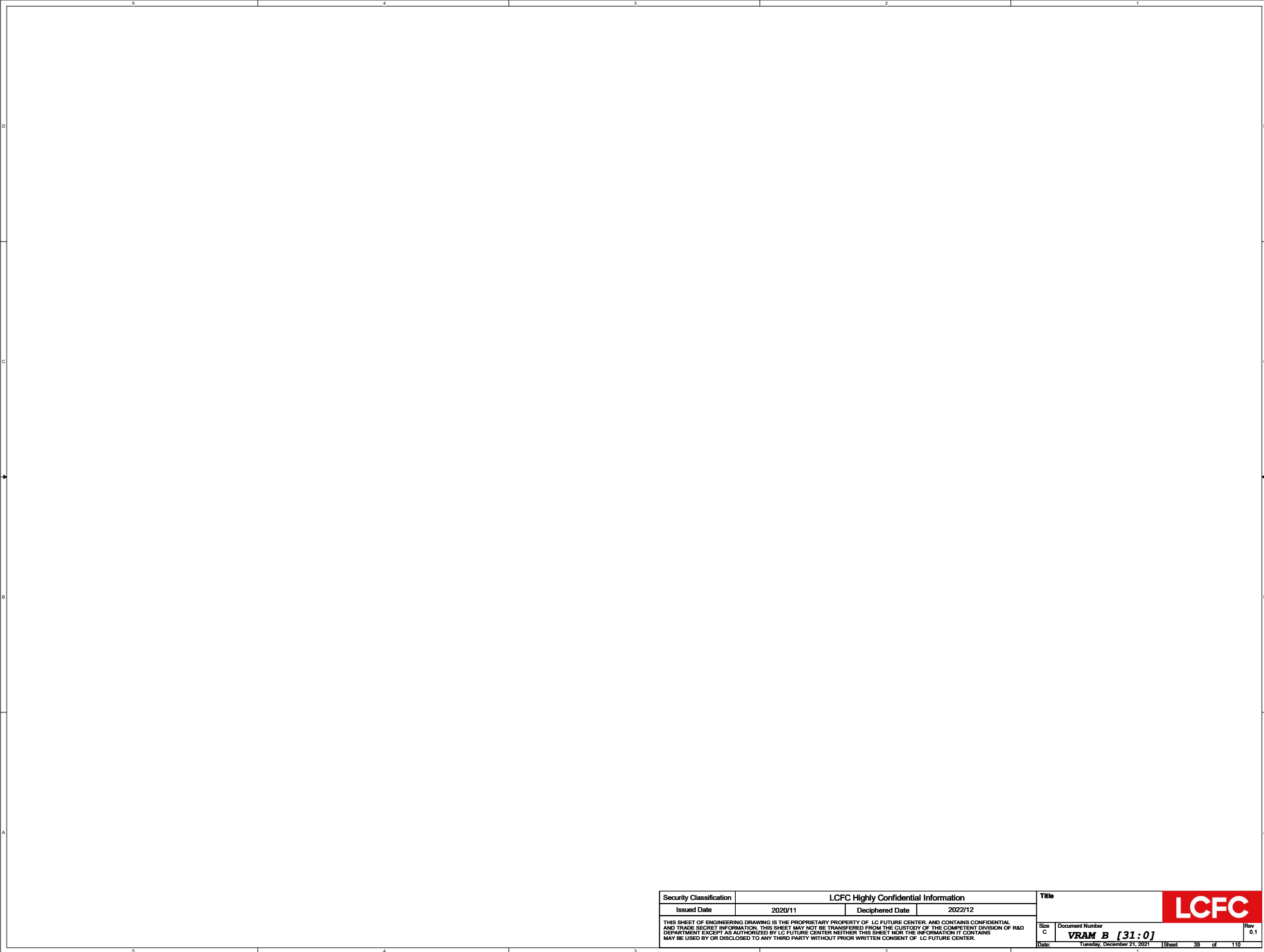
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Title			
Size	Document Number		
C	VRAM A [31:0]	Rev	0.1
Date:	Tuesday, December 21, 2021	Sheet	37 of 110




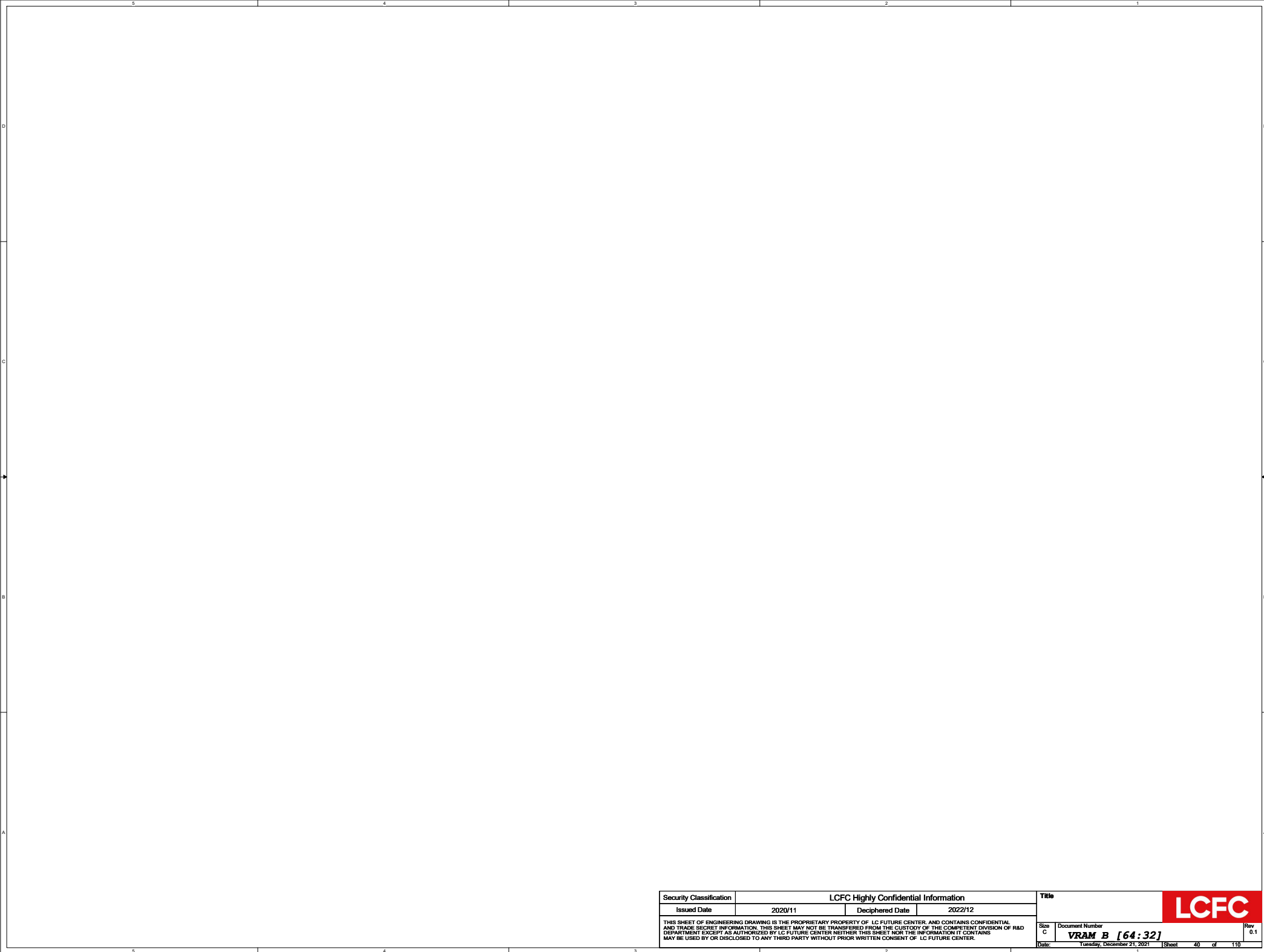
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Title			
Size	Document Number		
C	VRAM A [64:32]	Rev 0.1	
Date:	Tuesday, December 21, 2021	Sheet	38 of 110




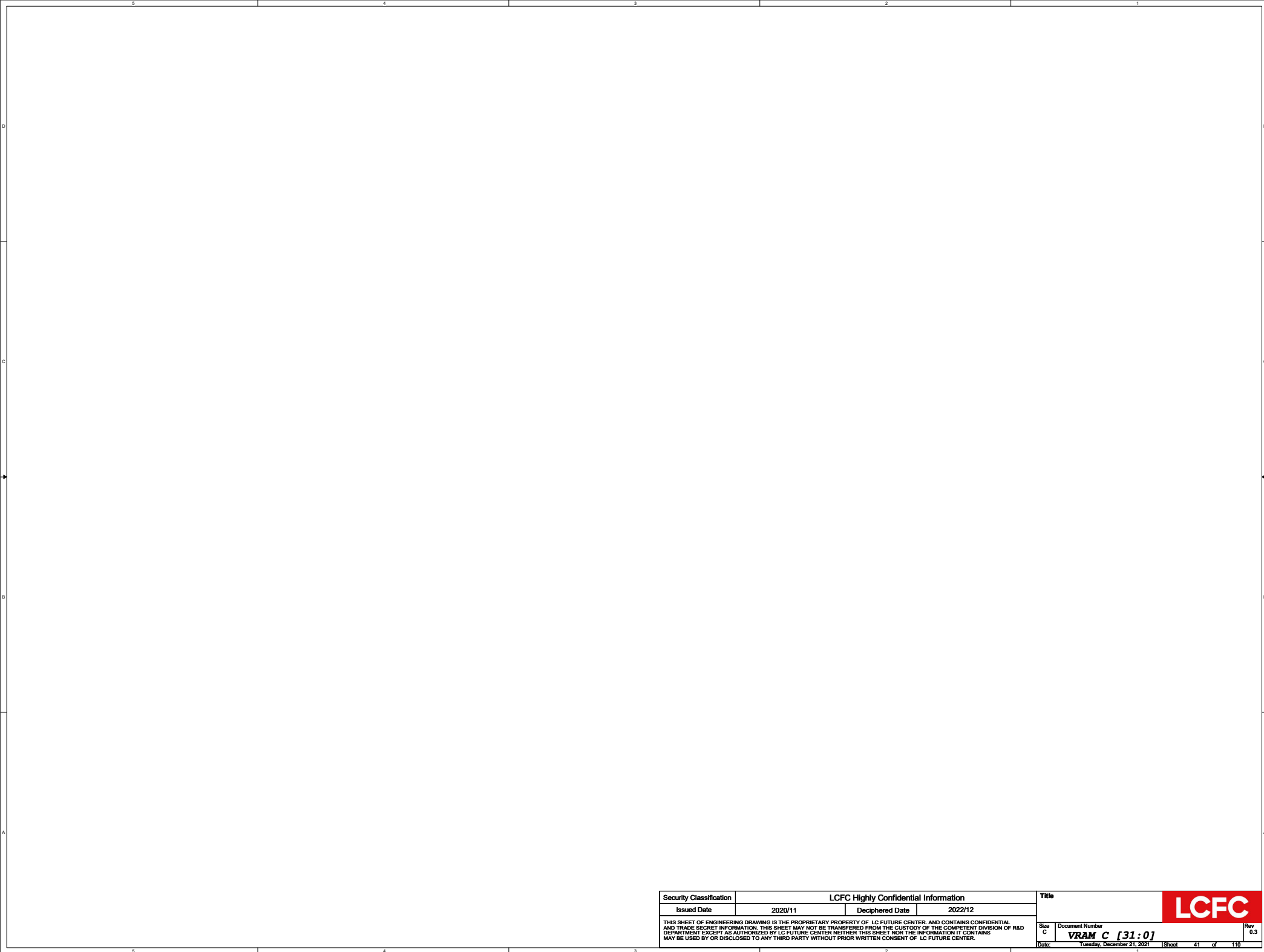
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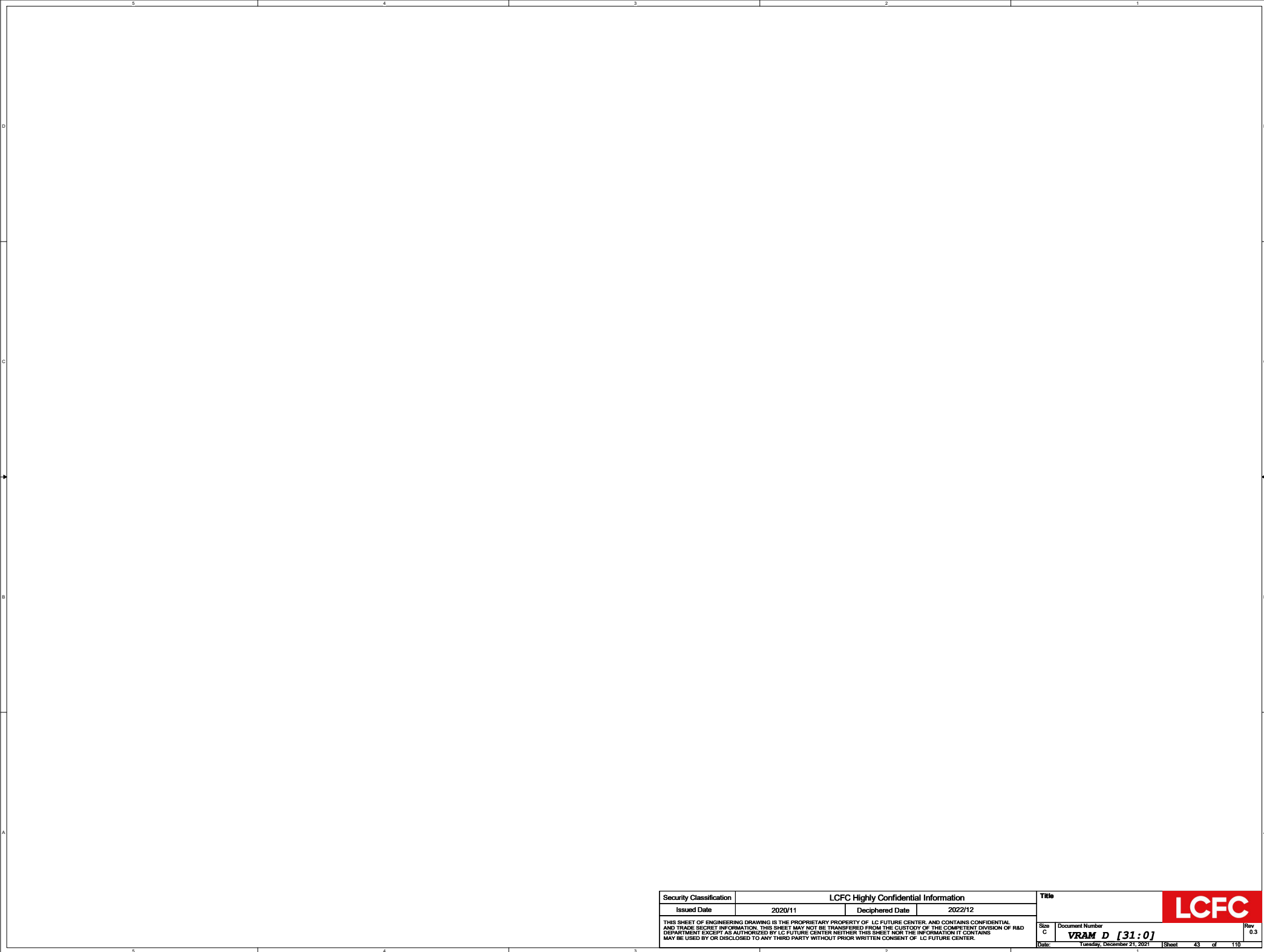
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C	VRAM C [64:32]	0.3	
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C	VRAM D [31:0]	0.3	
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C	VRAM D [64:32]	0.3	
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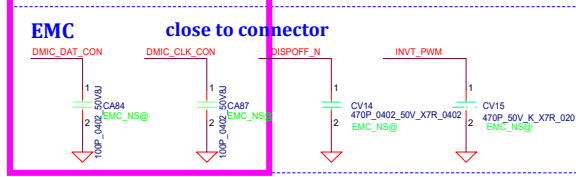
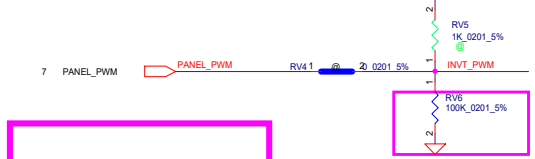
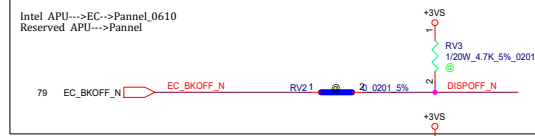
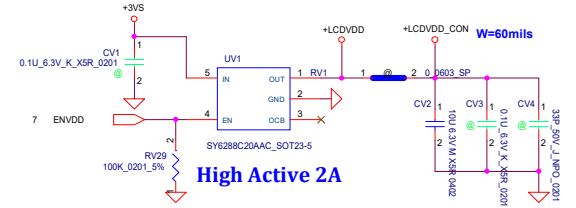
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C	NV DDS LOGIC	Rev	0.3
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LCD EDP Display

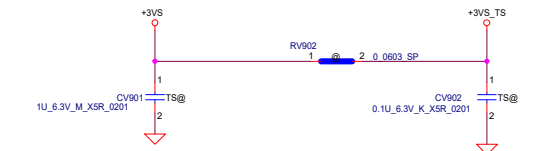
LCD Power Circuit

Follow Intel S360ITL_0610



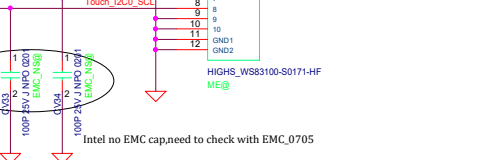
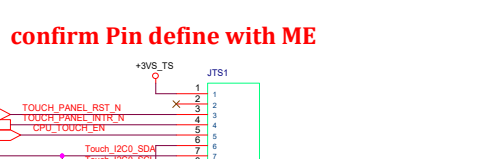
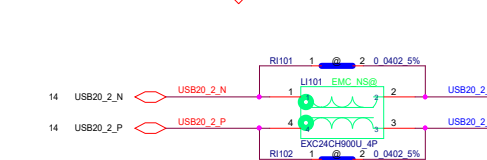
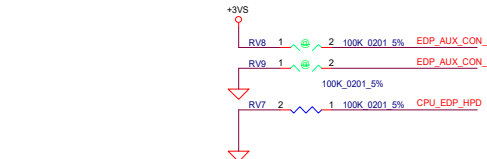
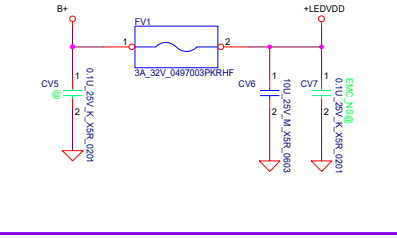
Touch Screen

Touch Panel Power_Follow s750_0705



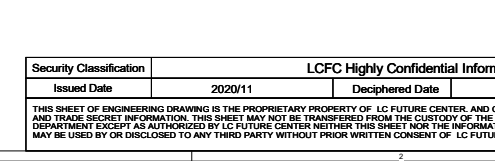
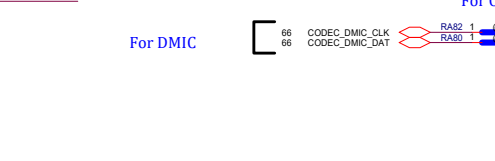
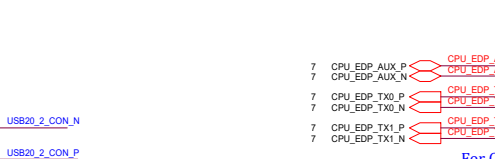
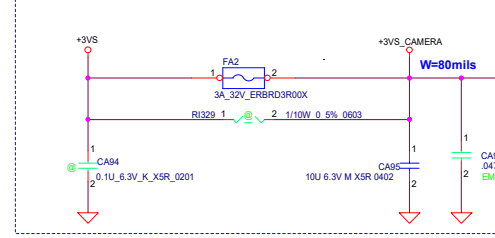
LED Power

Follow Intel S360ITL_0610

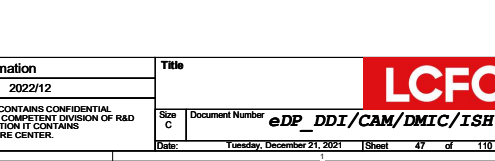
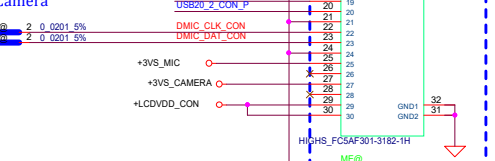
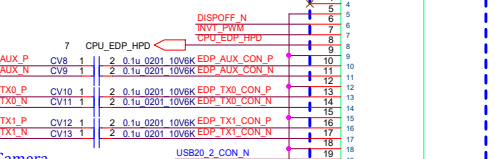
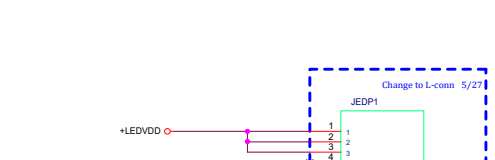
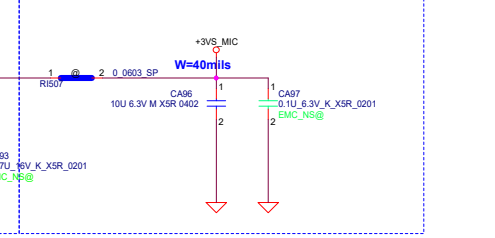


DMIC BOARD POWER

Camera



DMIC



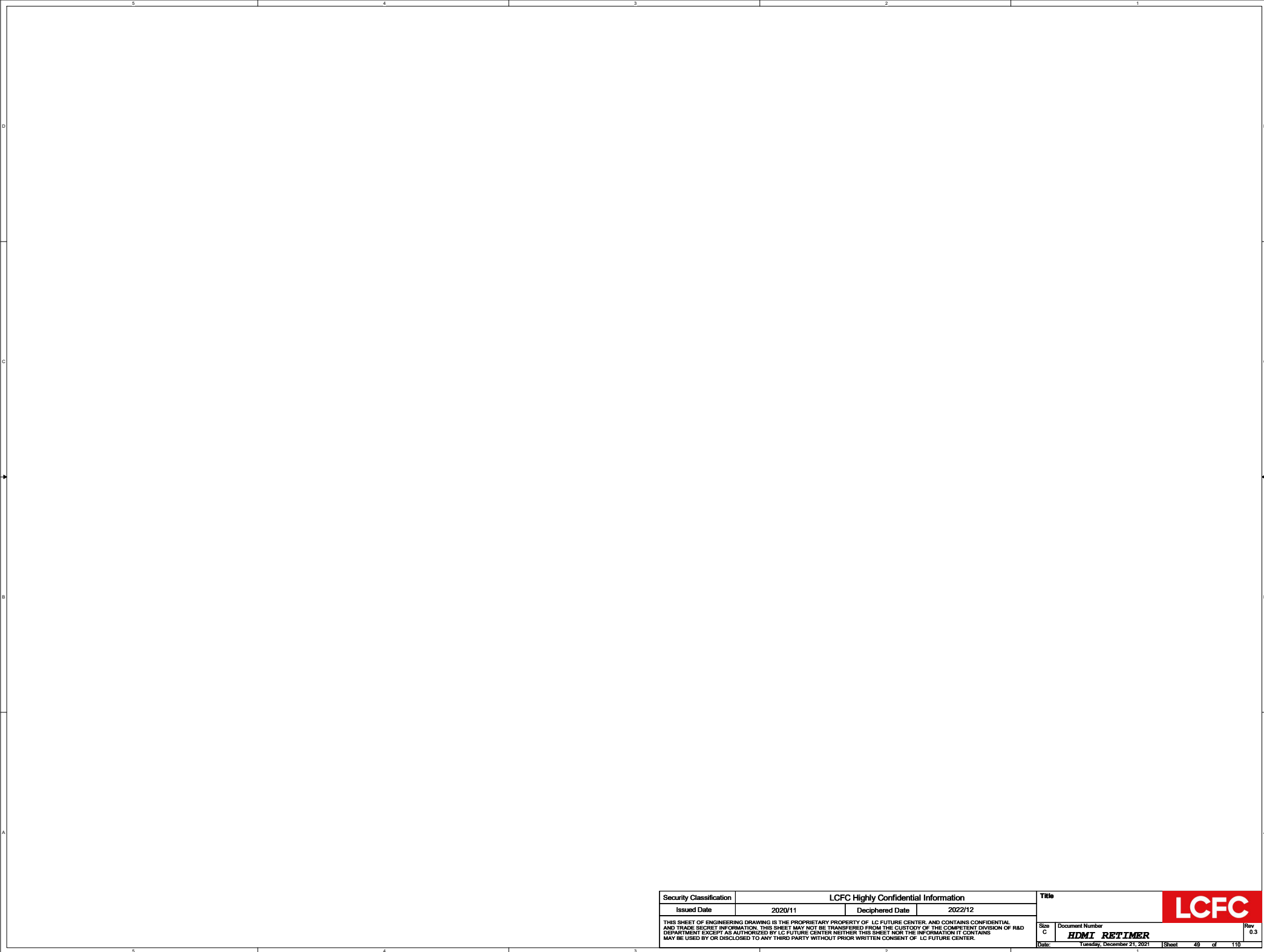
confirm Pin define with ME

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Date:																	Tuesday, December 21, 2021					Sheet		48		of		110	

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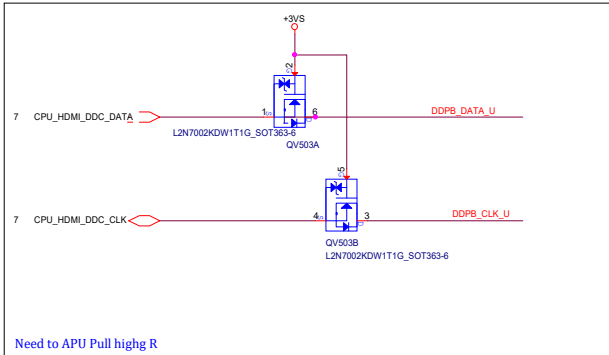
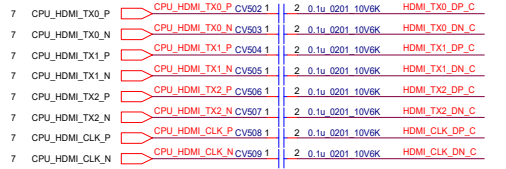
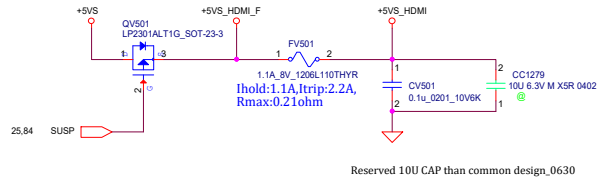


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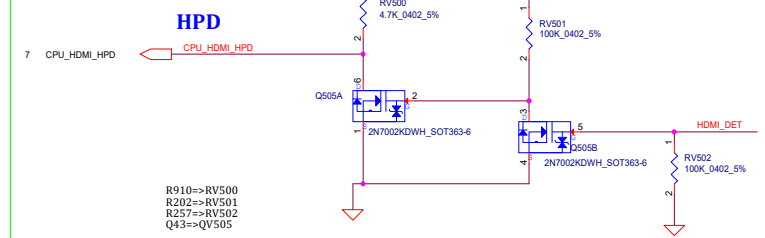
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Size	Document Number		Rev
C	HDMI RETIMER		0.3
Date:	Tuesday, December 21, 2021	Sheet 49 of 110	

Rev 0.3

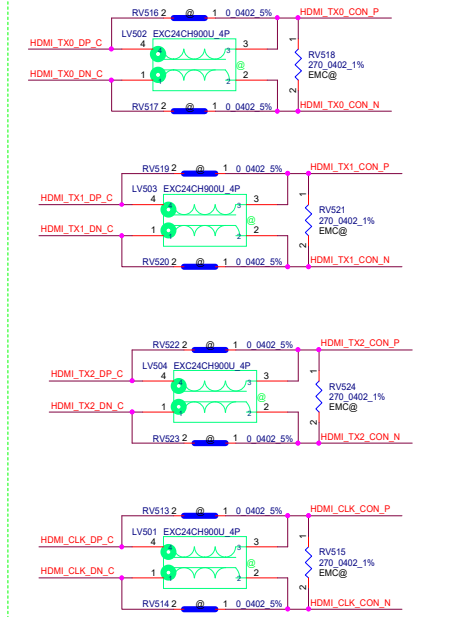
HDMI Power



Follwo Y550 A+N_0724

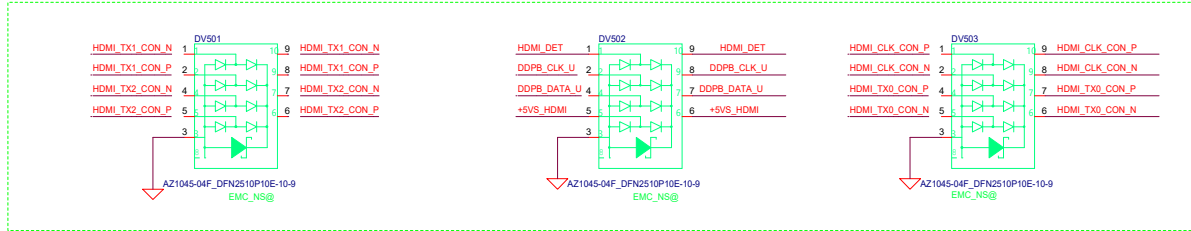


RV518,RV521,RV524,RV515,Follow.S50&550_ARE 270R

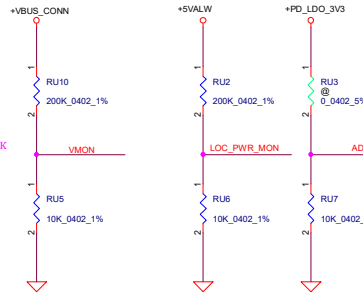


EMC

EMC



RTS5457V和RTS230进行Co-Lay,
5230的参考电路中RT5/RT6为20K,
是否也可以改为10K? 通过FW来配置?
两者都是ADC Input Channels,ADC
voltage range is different (1.2V~2.2V)
ITE: 分压可以和RTS5457V一样改为200K+10K



RA=RT3

RB=RT7

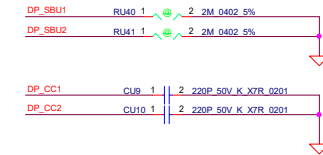
Slave Addr	Ra 5%	Rb 5%	
addr0:0xCC	NC	10K	<0.2V
addr1:0xCE	75K	10K	>=0.2V&&<0.6V
addr2:0xD0	33K	10K	>=0.6V&&<1.0V
addr3:0xD2	10K	10K	>=1.0V

It's is used for SMBUS slave addr0/1/2/3
setting during power on initialization

ITE: 5230时, RT39需改为0Ω---2021.06.21
If system support VBUS-IN power on

ITE建议初版仍采用0.1U+10U---2021.0618

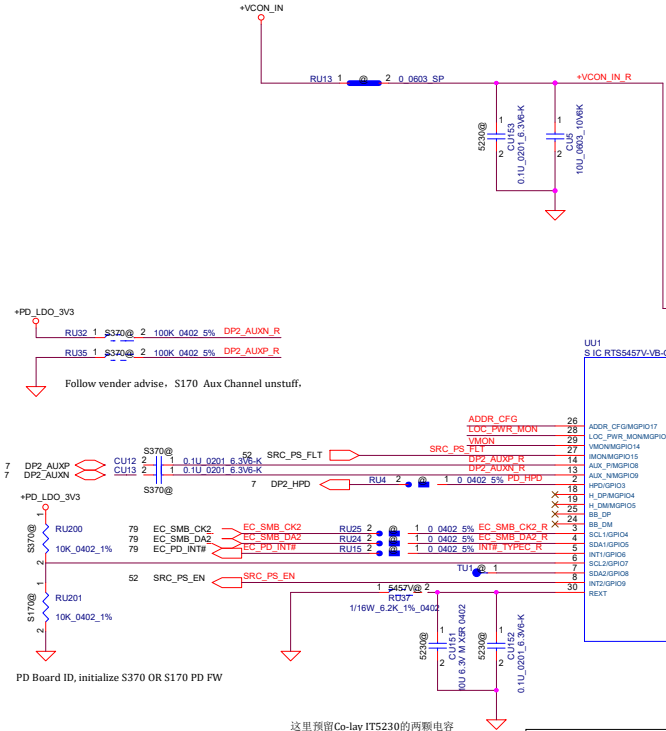
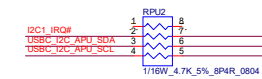
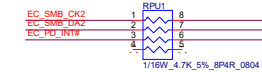
Follow PDG Require, add reserved 2M to GND_0811



RT30 Need to modify 2R_0805
RT30 Modify 2.2ohm 5% 0823 Follow S550

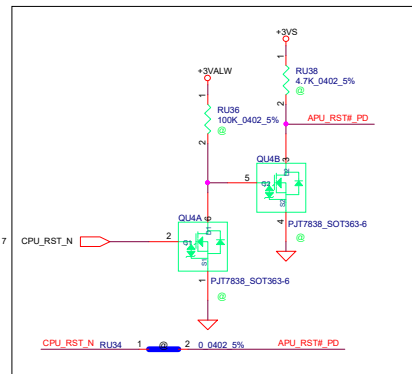
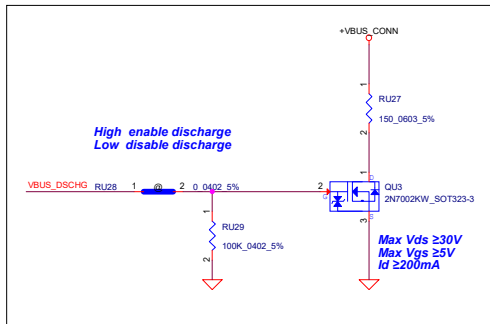
SRC_PS_EN RU9 1 2 4.7K 0402 5%

ITE5230的参考电路是2.2K上拉,
是否可以直接使用5457V的4.7K?
ITE: 根据实际应用后调整阻值



PD Board ID, initialize S370 OR S170 PD FW

这里预留Co-Lay ITS5230的两颗电容

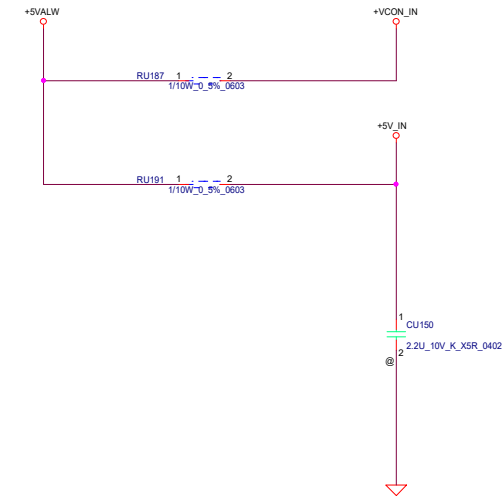
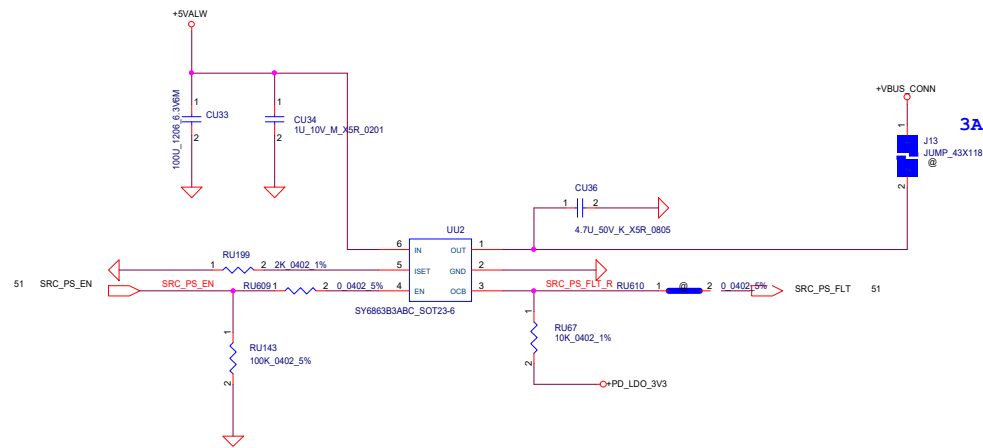


SA0000ACM00 NEW PN, Need to Program befor back !!!!
Use new material S IC RTS5457V-VB-GR QFN 40P CONTROLLER SA0000CQM00 _0830

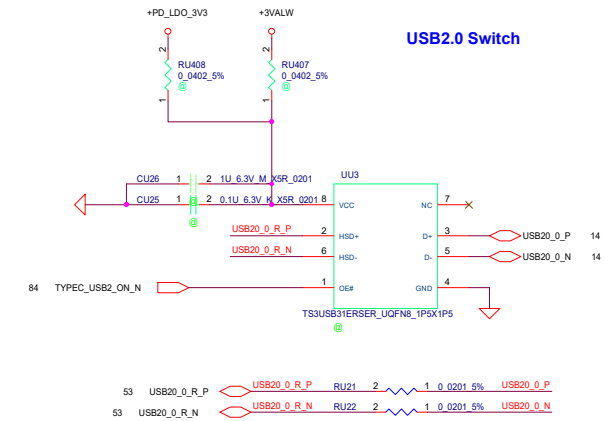
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				Date	110

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				Date	110

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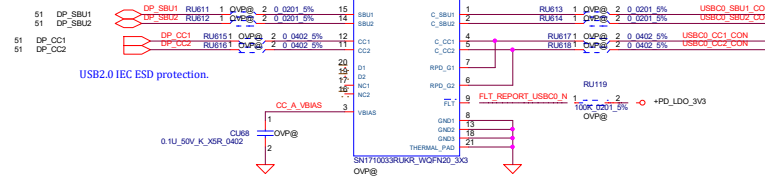


ADD Reserved LEO 0805



Follow S370_ADL

Follow S370_ADL

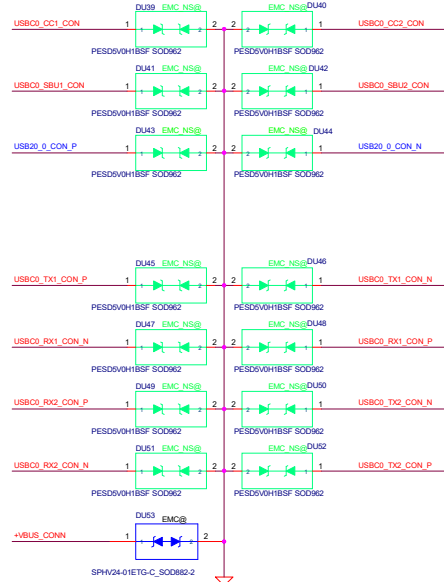



USB2.0 IEC ESD protection.

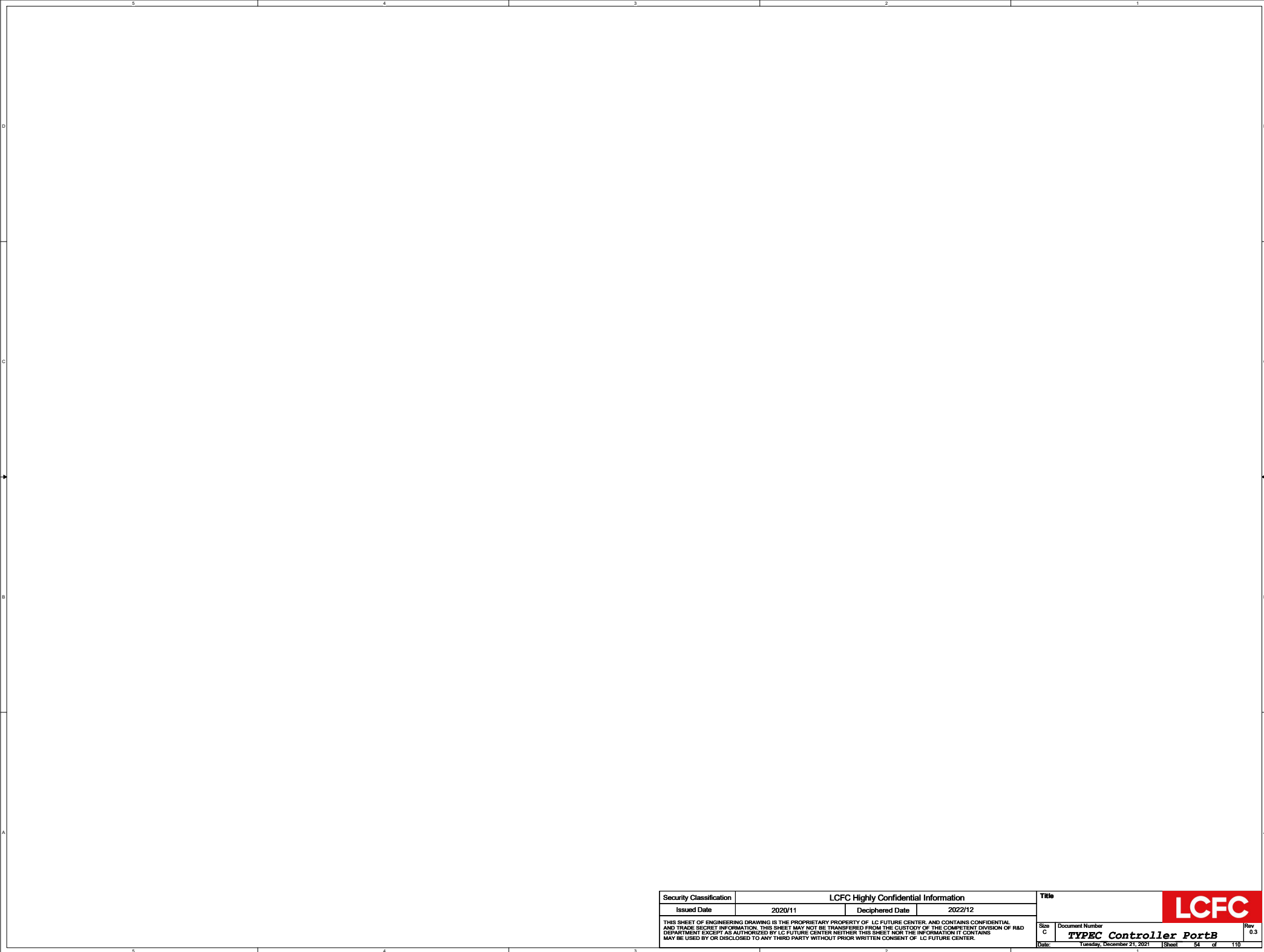
The schematic diagram illustrates the PUS401 driver circuit. It features a PUS401 MOSFET, an SP1224-01UTG-UDFN-6 optocoupler, and a 3S70 LED. The MOSFET is driven by the optocoupler's output. The LED is connected to the MOSFET's drain through a 0.1uF capacitor. The circuit is powered by a +VBUS_CONN supply and a 3.3V regulator. The MOSFET's gate is connected to the +VBUS_CONN supply through a 10k resistor. The MOSFET's source is connected to ground. The MOSFET's drain is connected to the LED's anode through a 0.1uF capacitor. The LED's cathode is connected to ground. The circuit is labeled 'PUS401 Change @ to 3S70@.0816'.

S170_ABA USE JUC1 ATOB_066-12A1-3211
Others USE JUC1 B200W 0823

S170_ABA USE JUC1 ATOB_066-12A1-3211
Others USE JUC1 B200W 0823

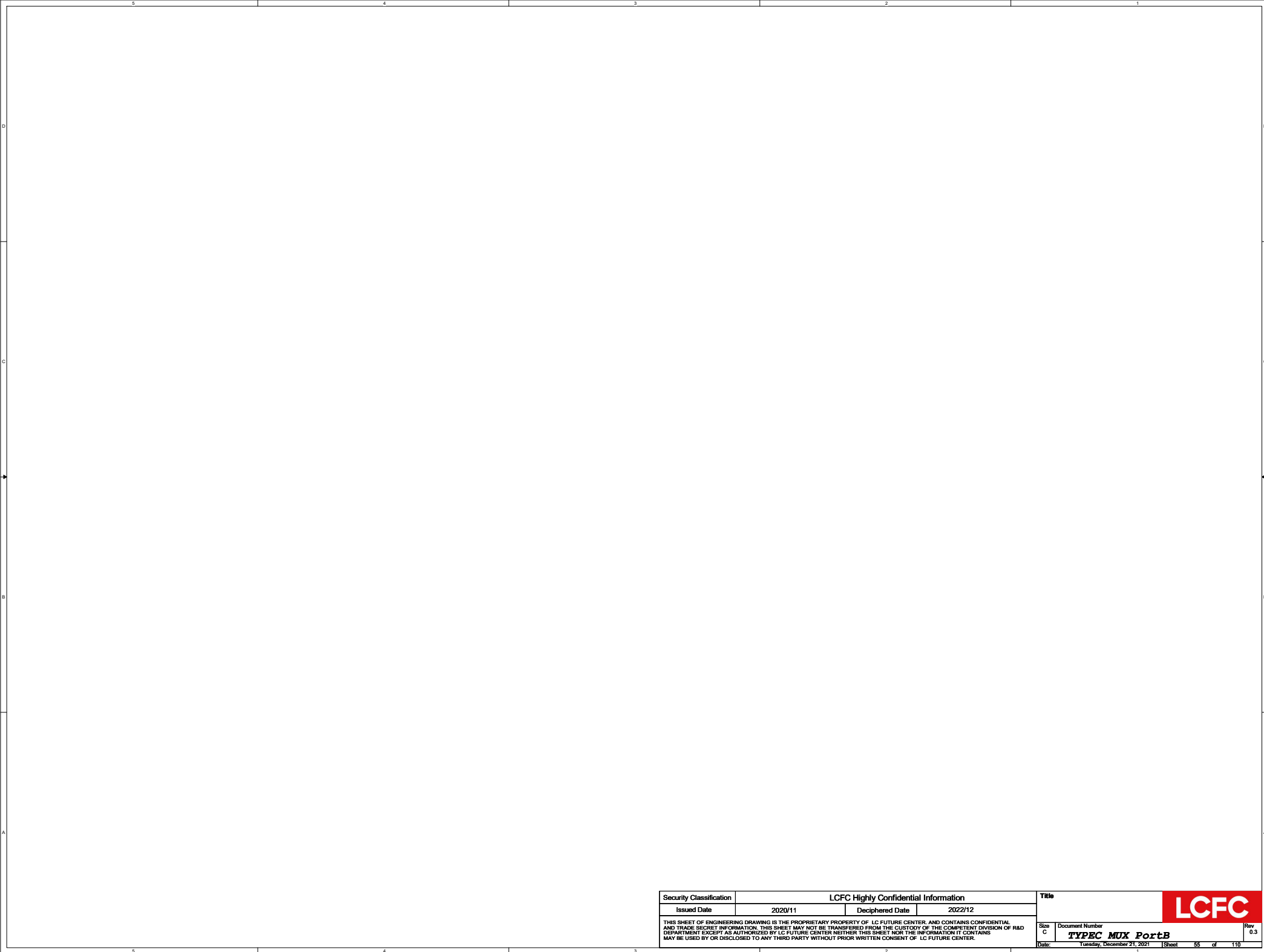
[illegible]

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Title			
Size	Document Number		
C	TYPEEC Controller PortB	Rev	0.3
Date:	Tuesday, December 21, 2021	Sheet	54 of 110

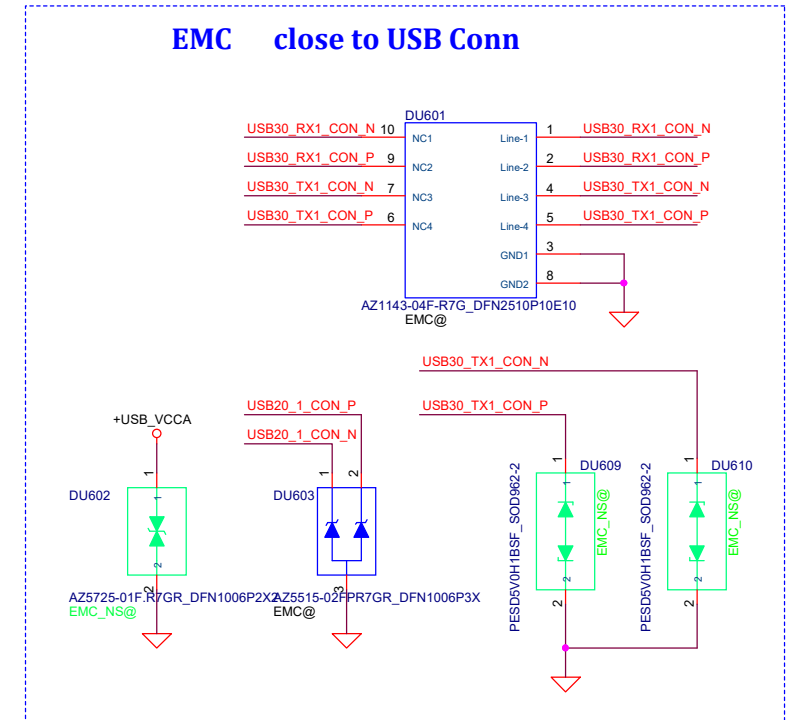
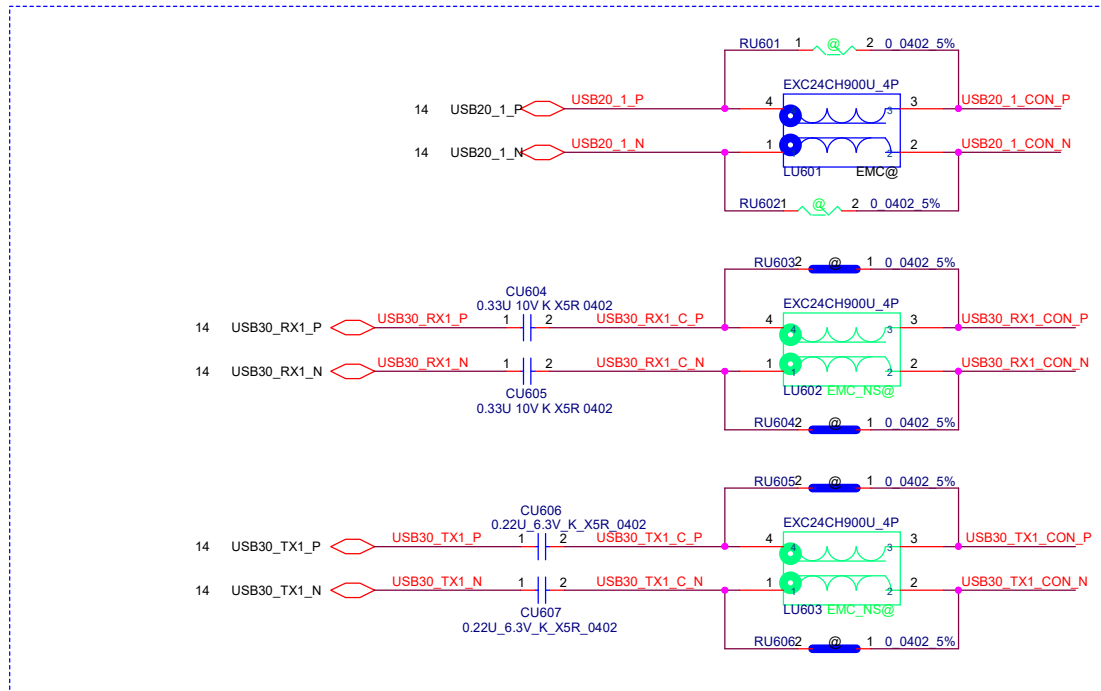
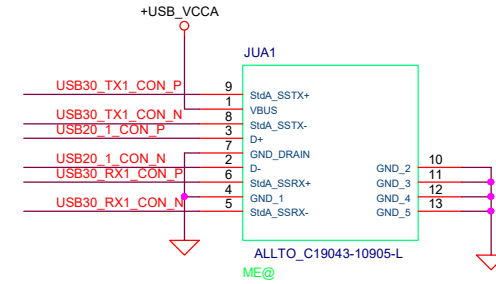
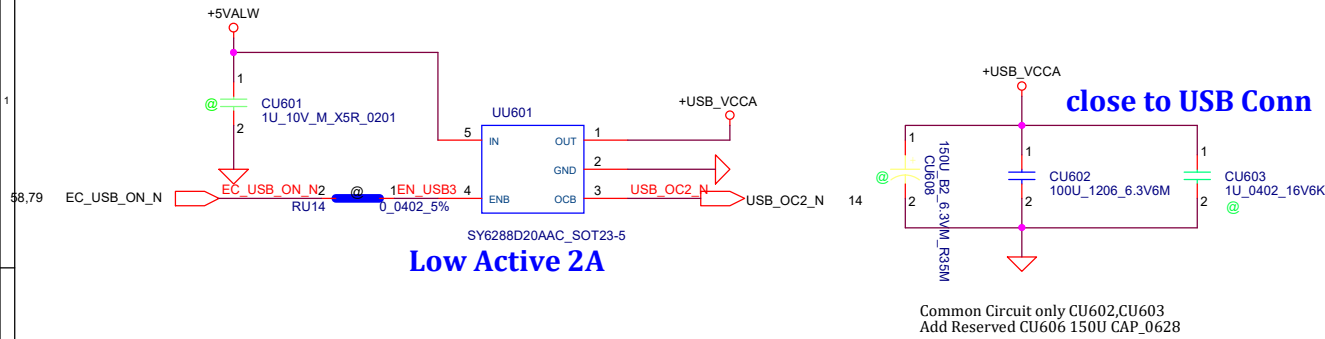


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Title			
Size	Document Number		
C	TYPEC_MUX_PortB	Rev 0.3	
Date:	Tuesday, December 21, 2021	Sheet	55 of 110

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				Custom		0.3
				Date		
				Tuesday, December 21, 2021		
				Sheet		
				56		
				of		
				110		

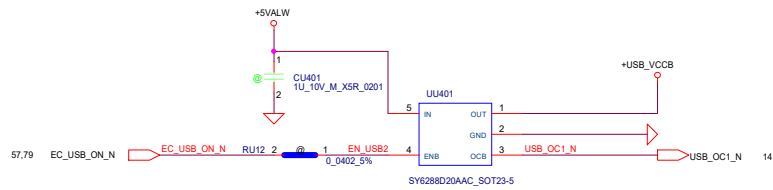
USB3.0 PORT



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Size B		Document Number				USBA Porta		Rev 0.3	
Date:		Tuesday, December 21, 2021				Sheet 57 of 110			


USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board

USB2.0 PORT



Low Active 2A

the different with Base:
1.S540 No USB2.0 only,S360&V14V15 have

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		USBA PortB				0.3
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Title			
Size	Document Number		
C	<i>USBA PortC</i>		Rev 0.3
Date:	Tuesday, December 21, 2021	Sheet 59 of 110	

Rev 0.3

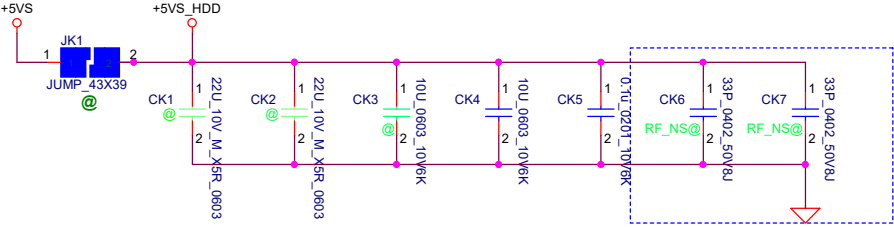


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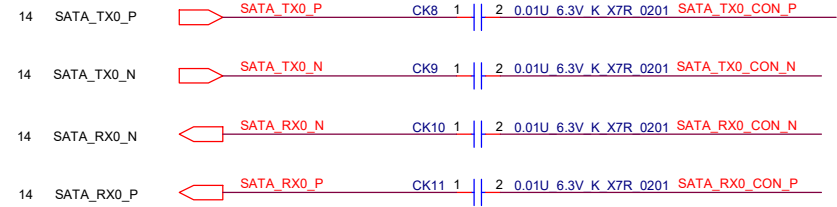
Title			
Size	Document Number		Rev 0.3
C	USB HUB		
Date:	Tuesday, December 21, 2021	Sheet 60 of 110	

Rev
0.3

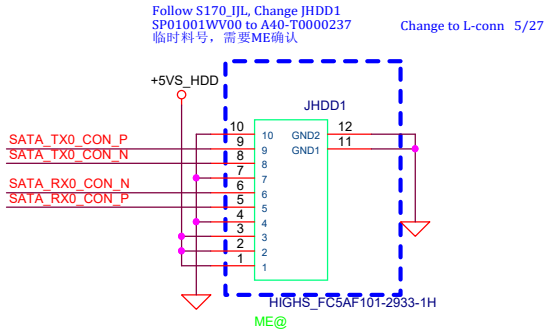
HDD Power



HDD Without Redriver



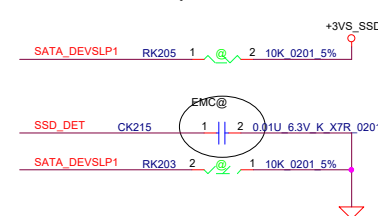
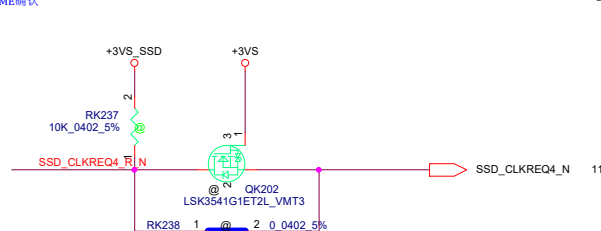
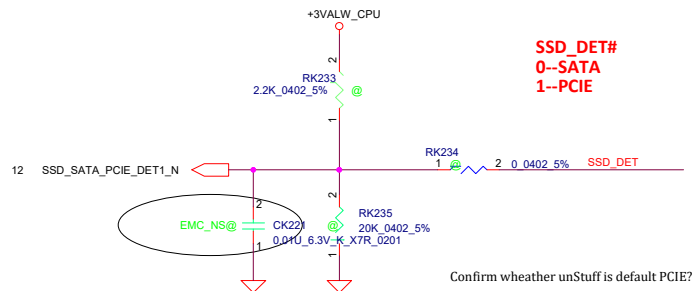
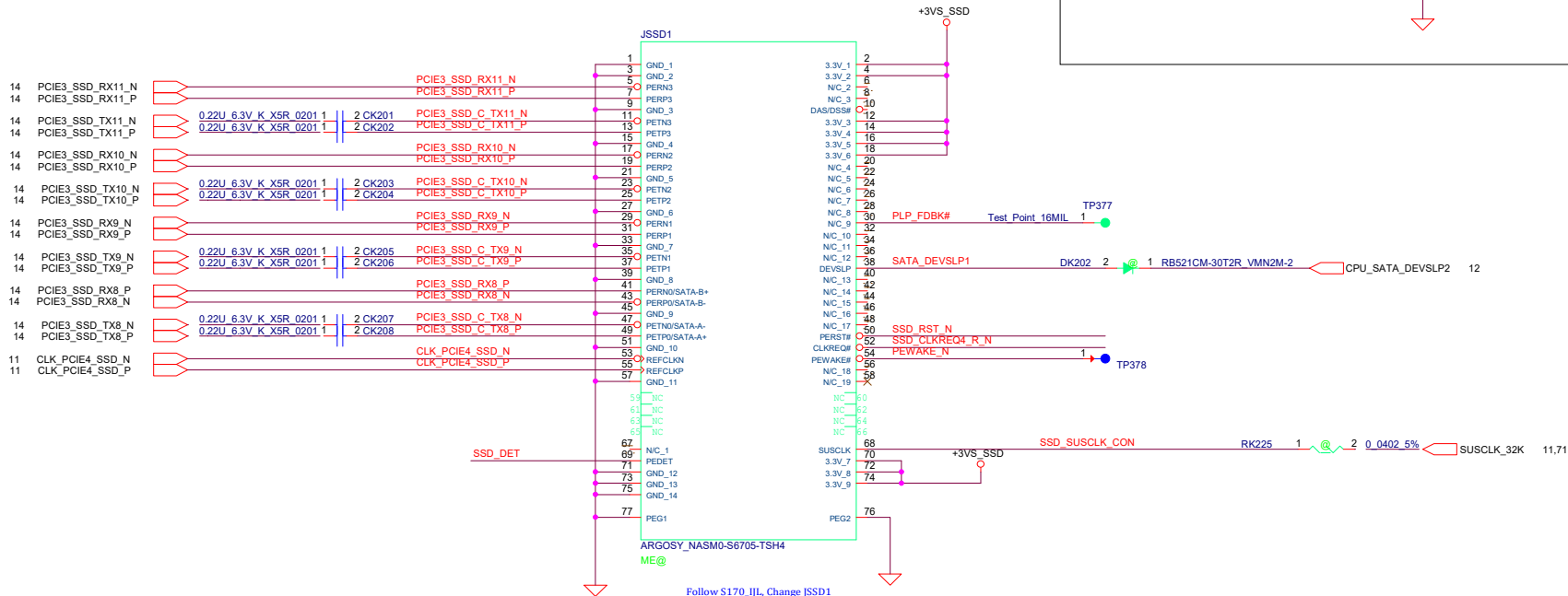
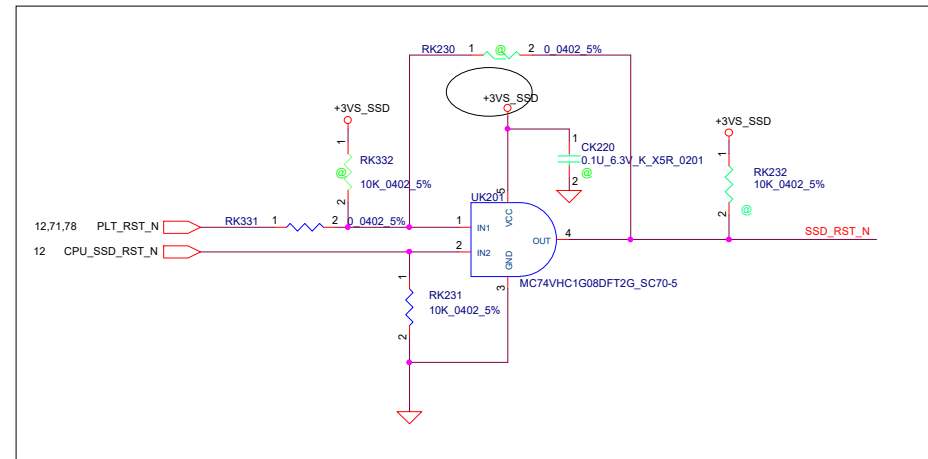
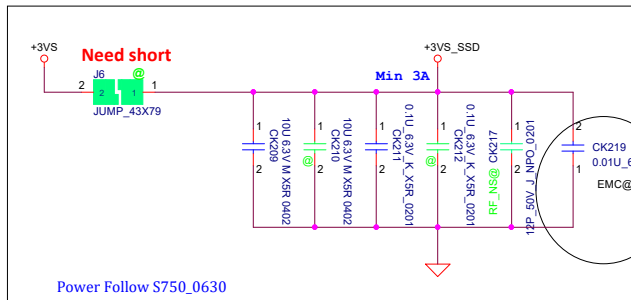
S370/170_ABL Delete HDD Redriver Design---2021.0616






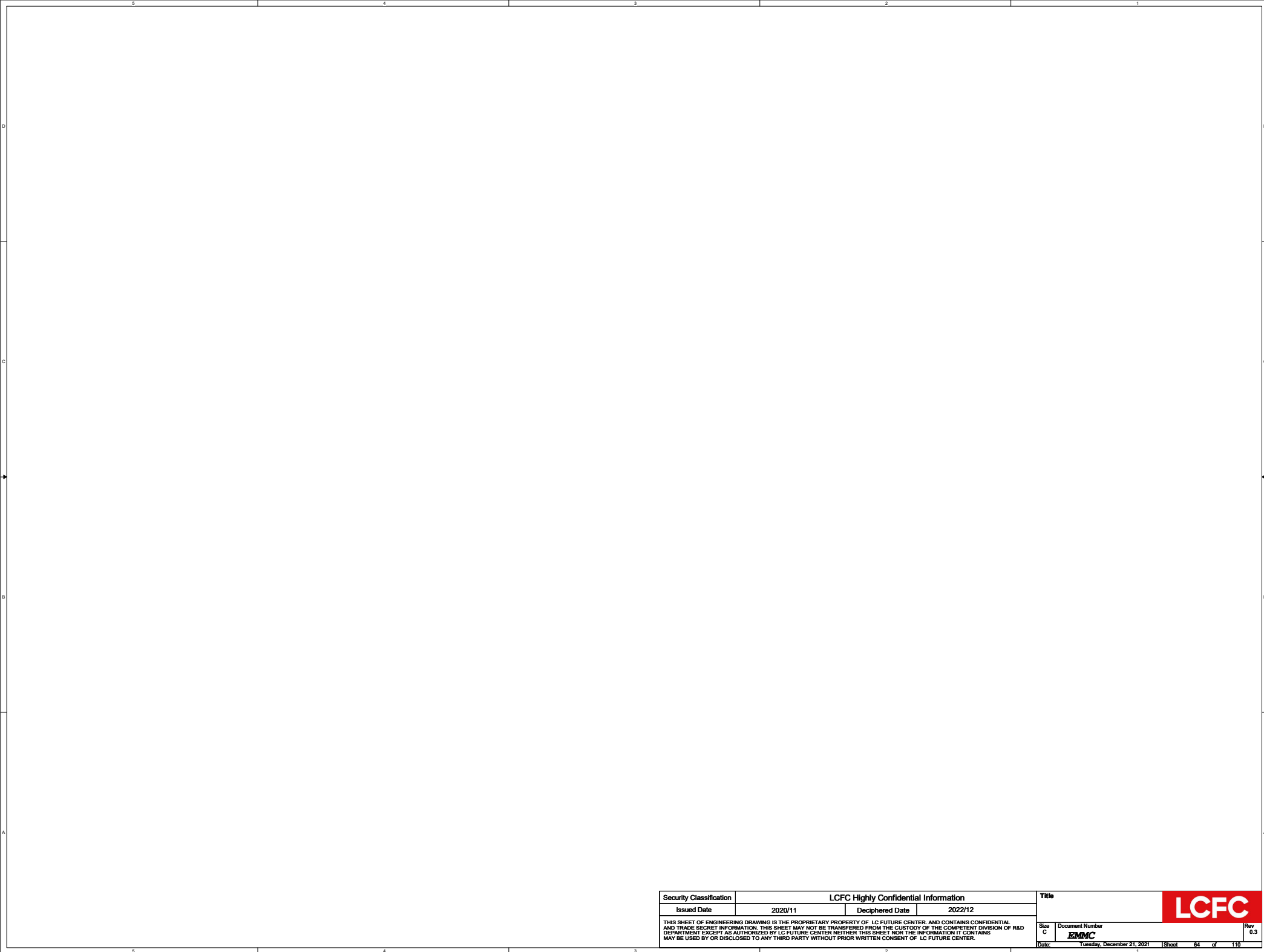
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Confirm wheather unStuff is default PCIE?

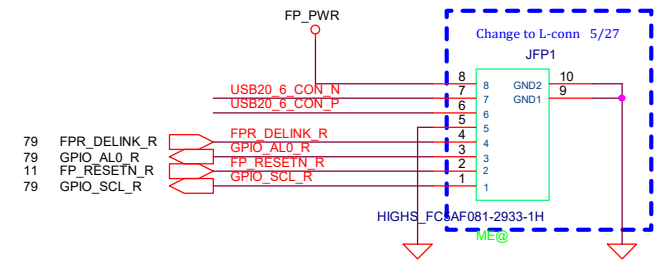
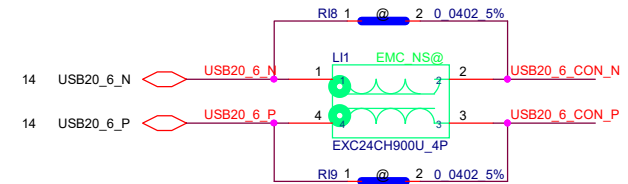
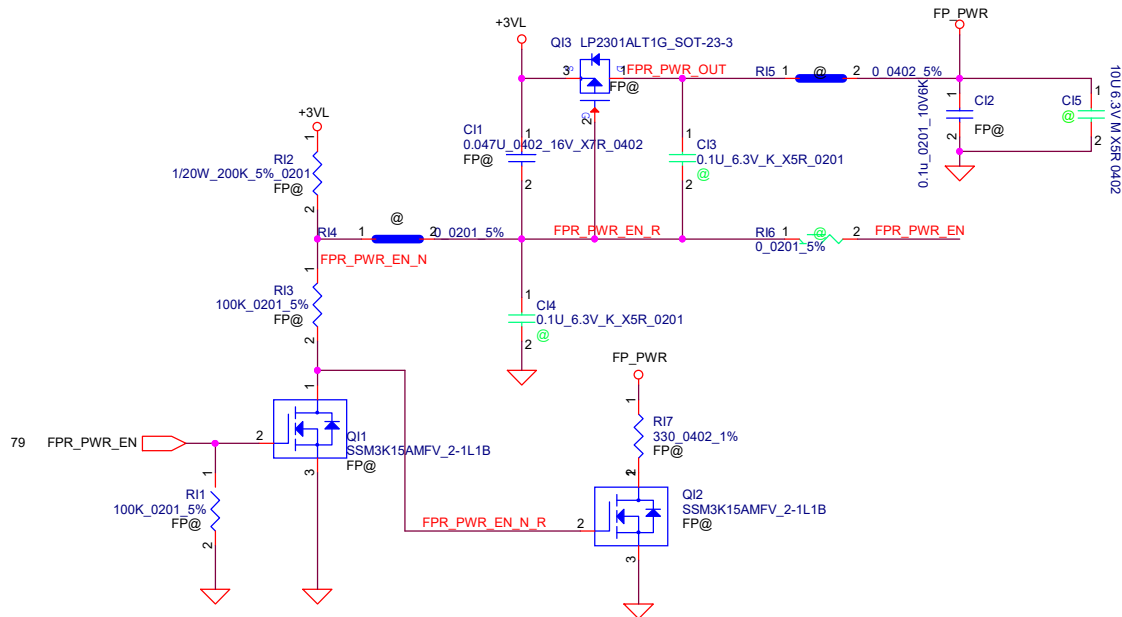
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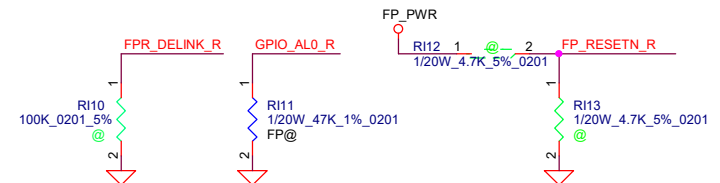
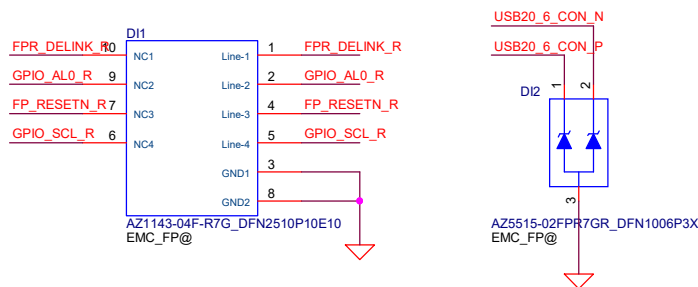
Title			
Size	Document Number		
C	EMMC	Rev 0.3	
Date:	Tuesday, December 21, 2021	Sheet	64 of 110

FP Power Control



Follow S170_IJL, Change JFP1
SP01001YV00 to A40-T0000240
临时料号, 需要ME确认

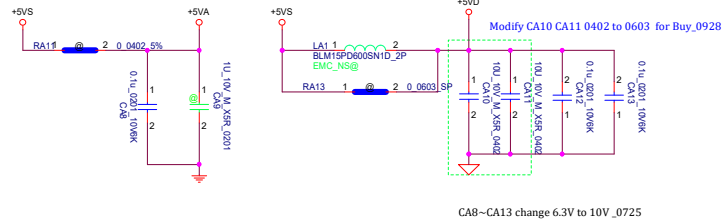
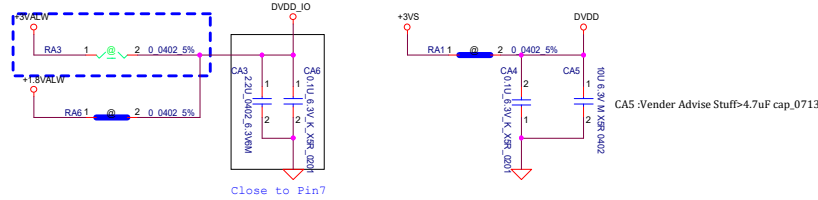
EMC close to Conn



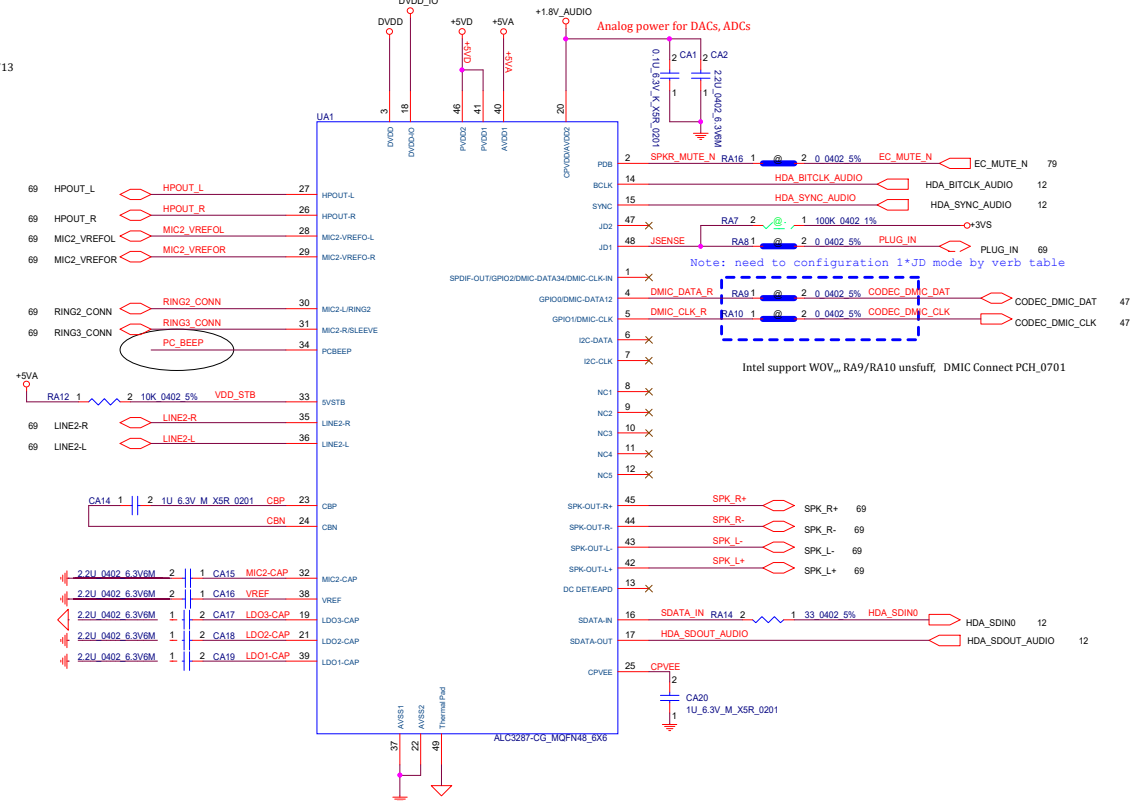
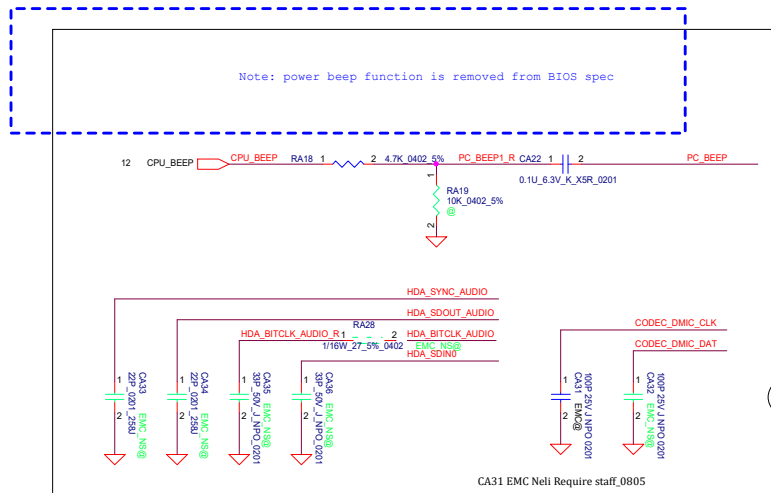
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Date:		Tuesday, December 21, 2021		Sheet	65	of 110

the diffrent with Base MODULE:
1.Module no ra3 to DVDD_IO,S360&V14&V15 reserve
2.Module no ra5 CA21 to EC_BEEP,S360&V14&V15 reserve

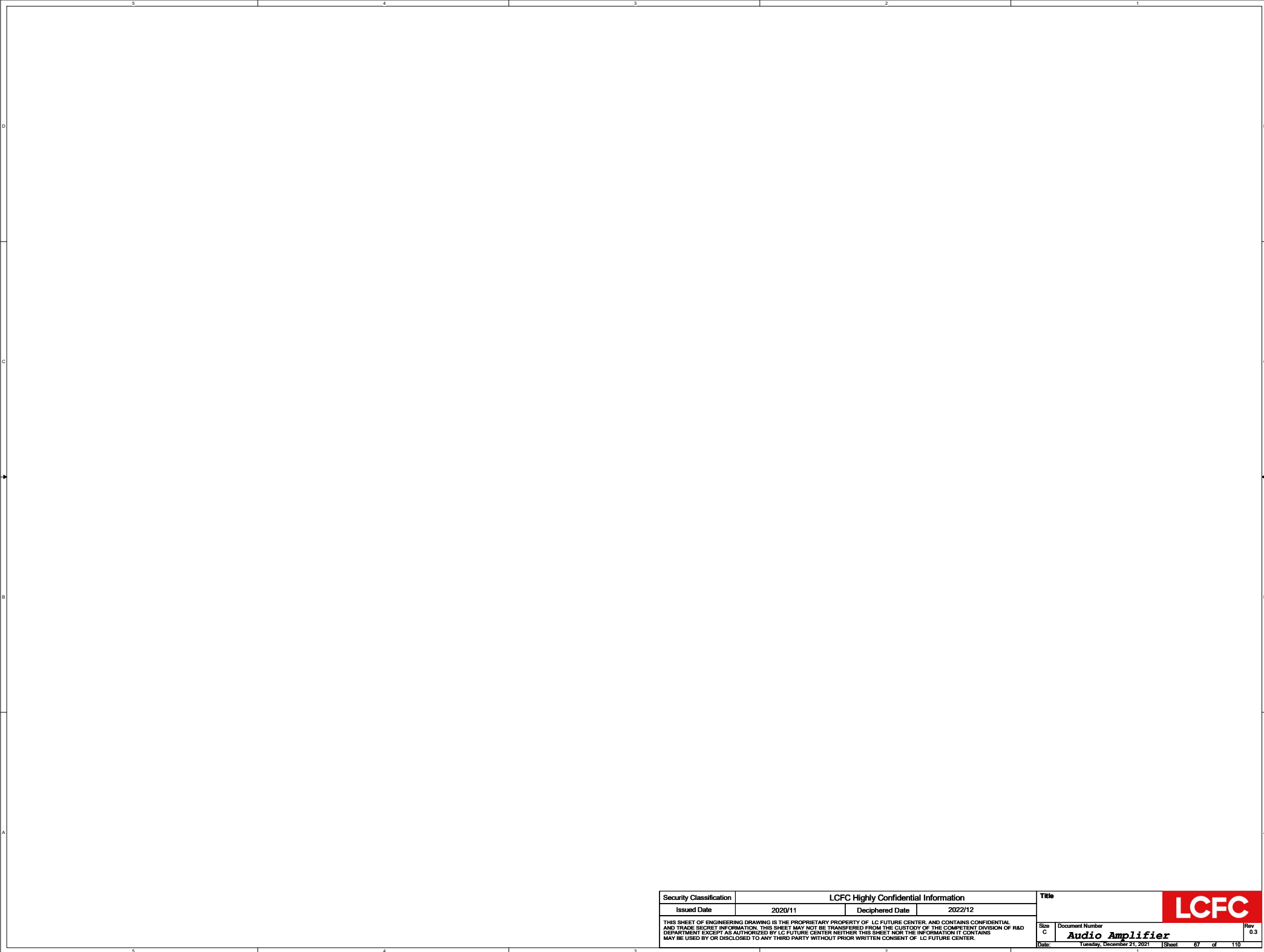
Note: DVDD-IO must be equal to or smaller than DVDD



Follow Intel, beep need to confirm_0701



CA91, CA92 Is it necessary to reserve



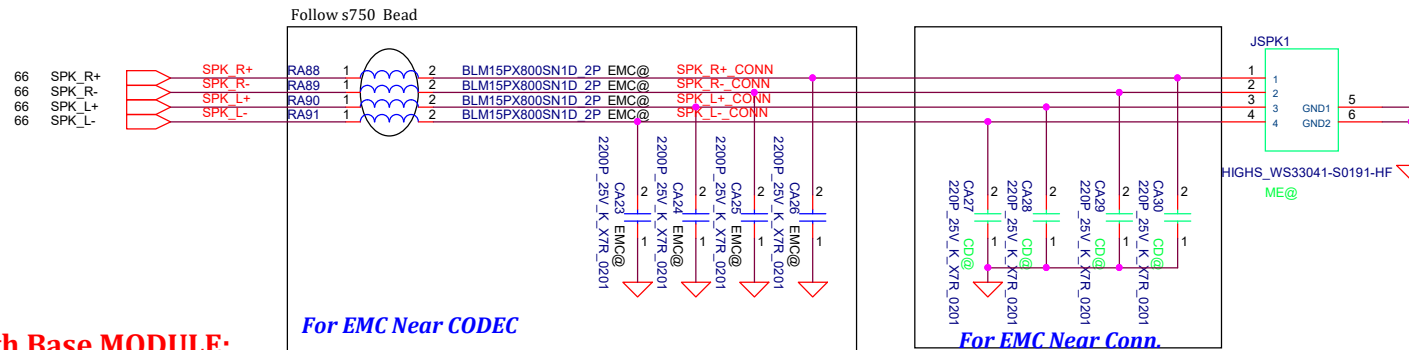
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Title			
Size	Document Number	Rev	
C	Audio Amplifier	0.3	
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Title			
Size	Document Number		
C	Audio DSP	Date:	Rev
Tuesday, December 21, 2021		Sheet	0.3
1		68	110



Speaker

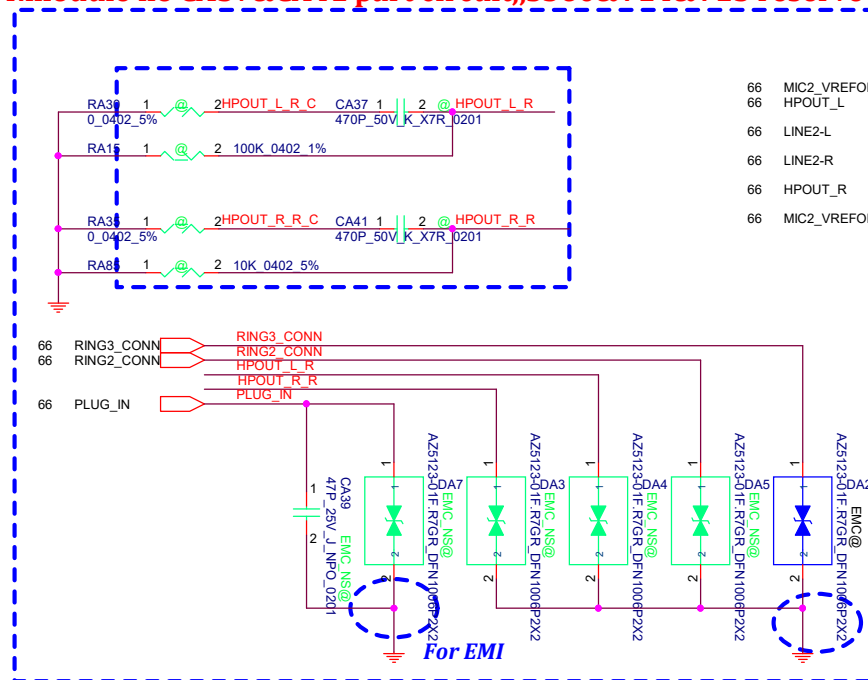
the different with Base MODULE:

1.S360&V14&V15 RA86&RA87 VALUE different with module,

2.for EMC TVS EMC_NS@ type different with module

3.GND type different

4.module no CA37&CA41 part circuit,S360&V14&V15 reserve



Audio Jack

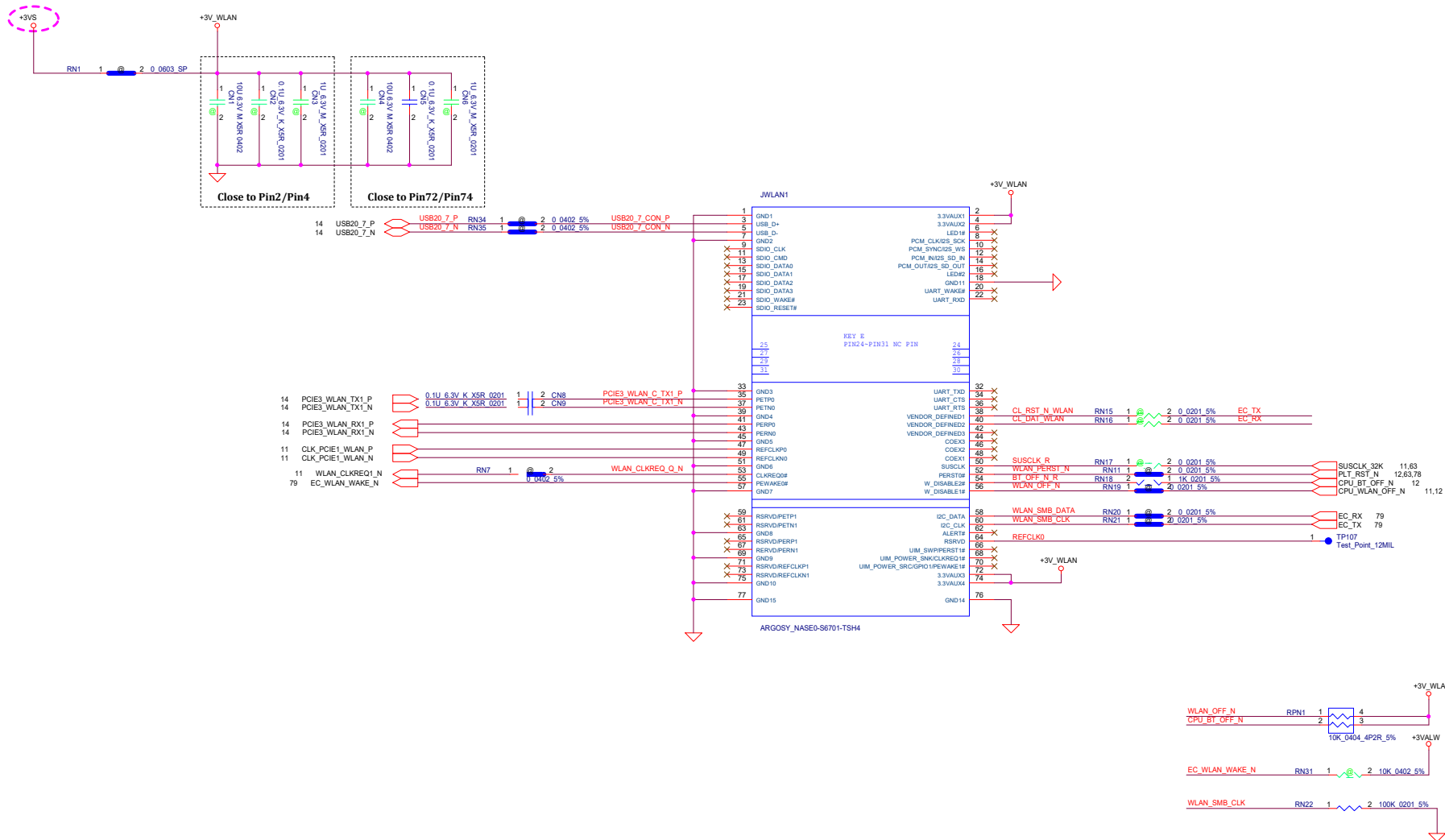
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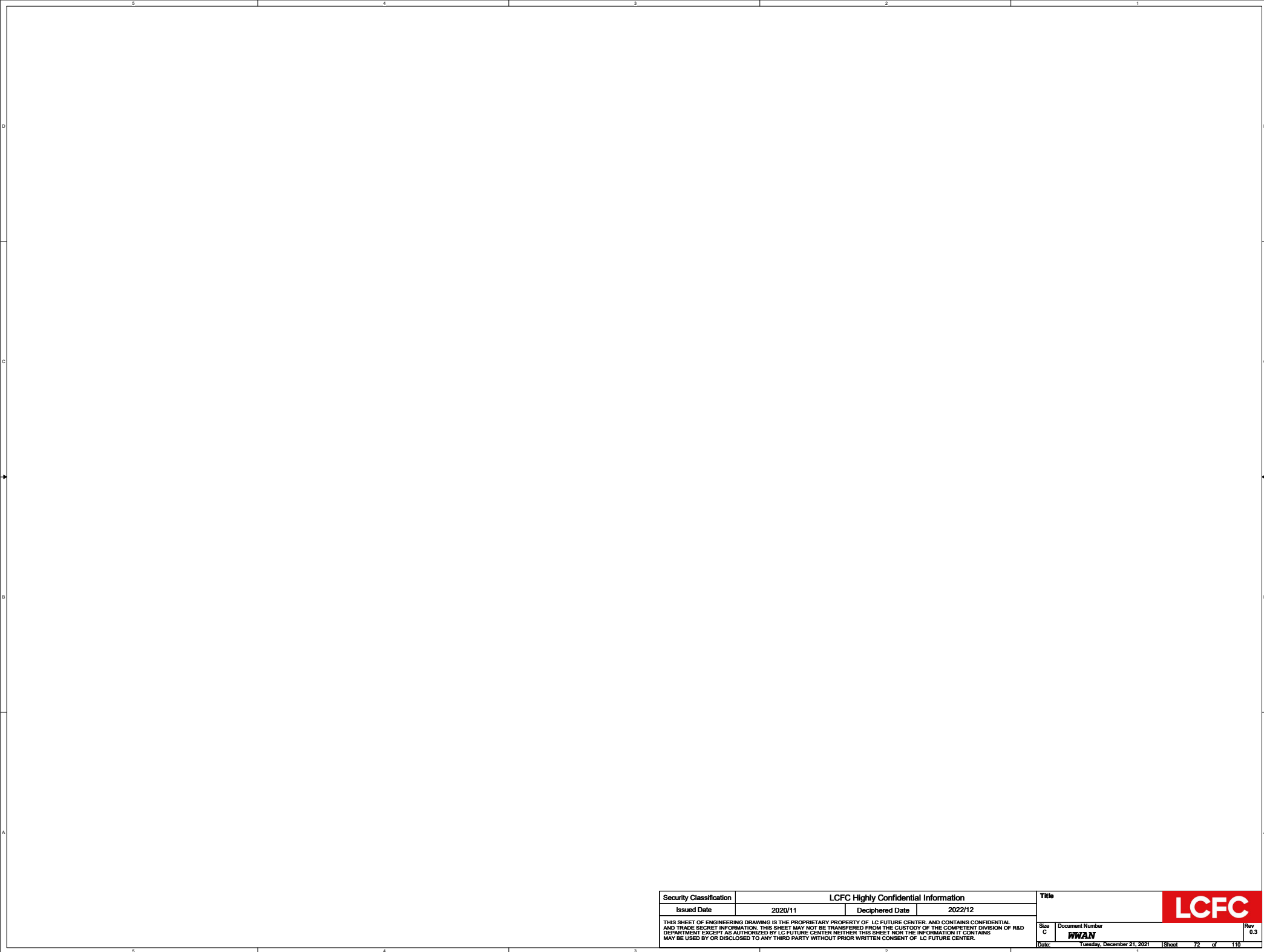
Audio SPK/Jack

S360_AUC
Card reader Circuit MOVE to SUB Board S360
USB2.0 on SUB Board

Copy Wlan common design




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Title			
Size	Document Number		
C	WWAN	Date:	Rev
Tuesday, December 21, 2021		Sheet	0.3
1		72	110
		of	

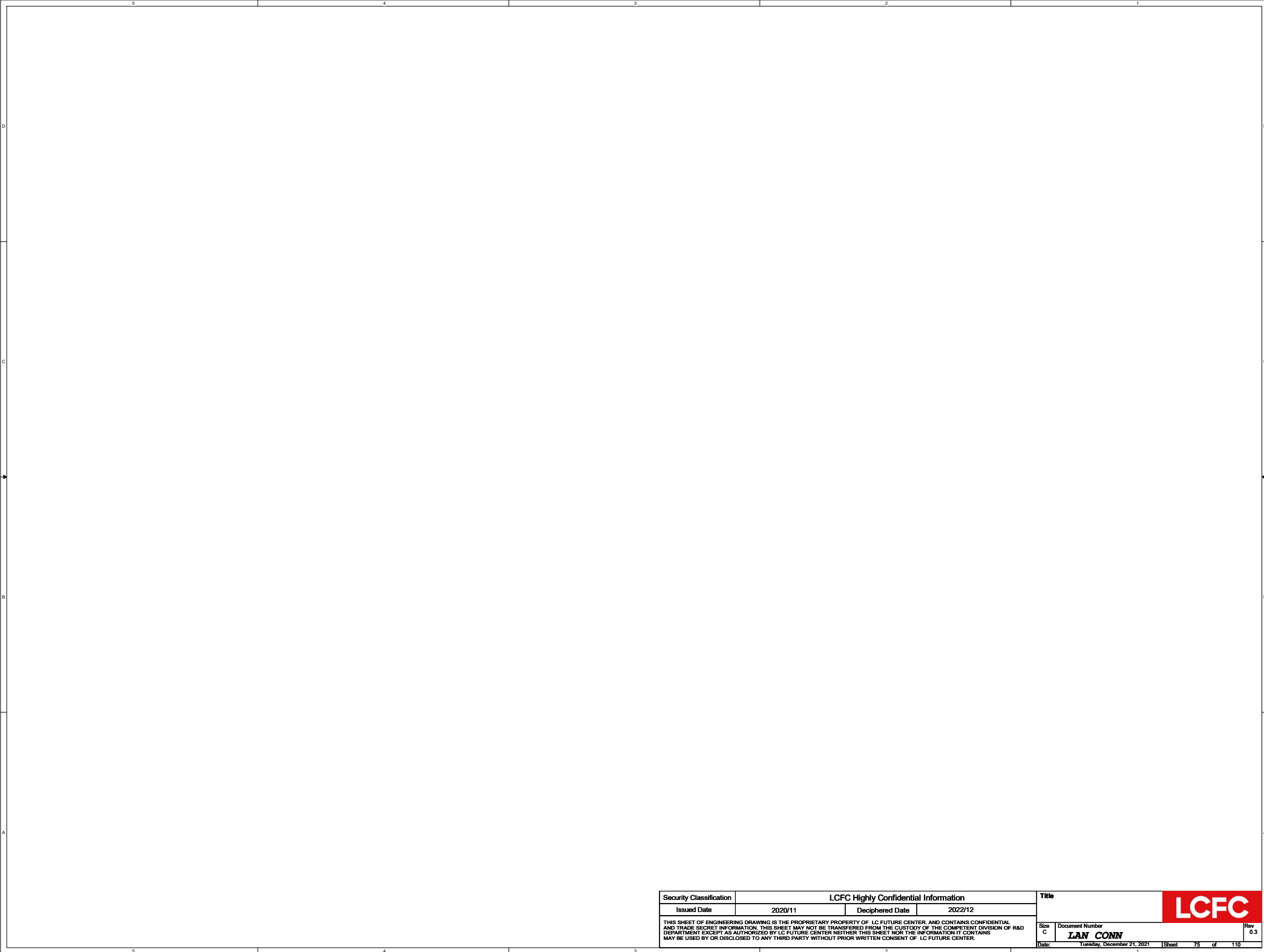
LAN Circuit MOVE to SUB Board in V360 DB V14V15

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				Date:	Tuesday, December 21, 2021	Sheet	73 of 110



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Title			
Size	Document Number		
C	LAN Transformer	Rev	0.3
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Title			
Size	Document Number		
C	LAN CONN	Date:	Rev
Tuesday, December 21, 2021		Sheet	75 of 110

A

USB2.0_1 For USB2.0 Connector;
USB2.0_6 For S360 Card Reader

S360 ALC AMD Record

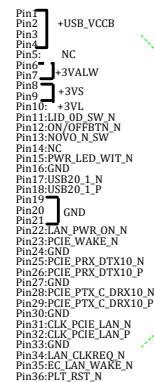
IO CONN

IO小板上的Pin名字沿用S170-IJL的，但是USB信号以及PCIE信号实际Port口需要看MB上的信号名：

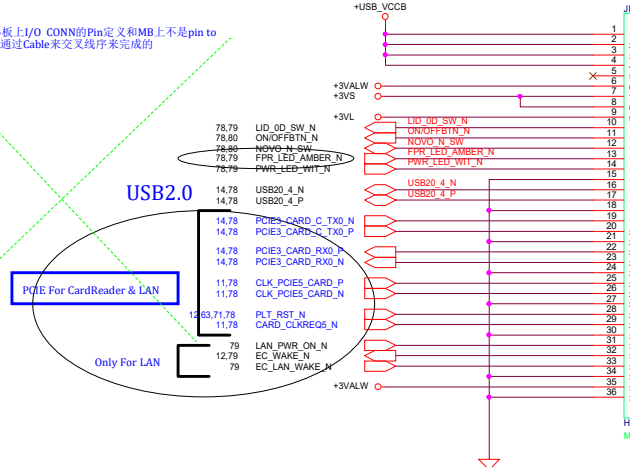
USB2.0_4 For USB2.0 Connector;

V14V15: USB2.0 LAN

V14V15 IO CON Pin define

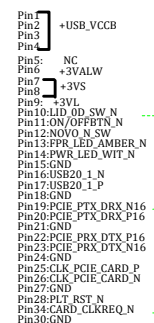


V1415的小板上I/O CONN的Pin定义和MB上不是pin to pin的,而是通过Cable来交叉线序来完成的

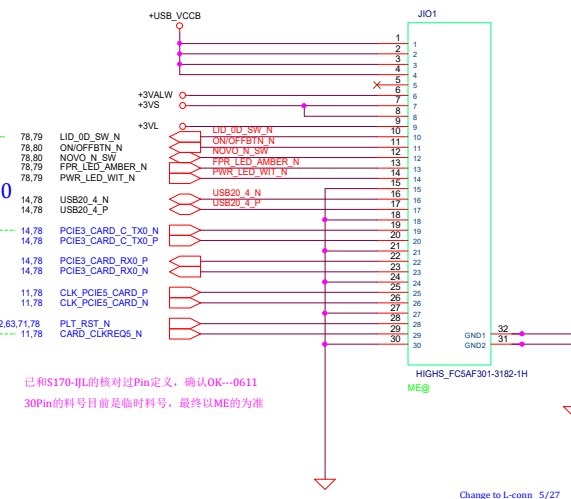


S170S370: USB2.0 CardReader

S370/170 IO CON Pin define



S370/170的小板上IO CONN的Pin定义和MB上是pin to pin的，通过Cable直接连线来完成的。

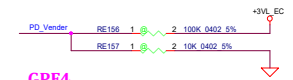


已和S170-IJL的核对过Pin定义，确认OK---0611

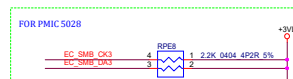
30Pin的料号目前是临时料号，最终以ME的为准

Change to L-conn 5/27

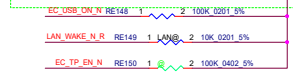
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Size	Document Number Sub Board CONN			Rev 0.3
Date	Issued: December 21, 2021 13:50:00 78 of 110			



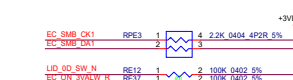
ADD Reserved PD Vender Judg



EC_U



Reserve PD_VIN_CTRL, Follow S550



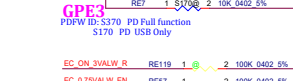
GPD1 Follow Intel s360 ITL



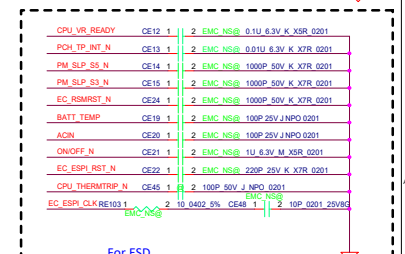
ALW_PWRGD is +3VALW_PWRGD_0



intel_0707

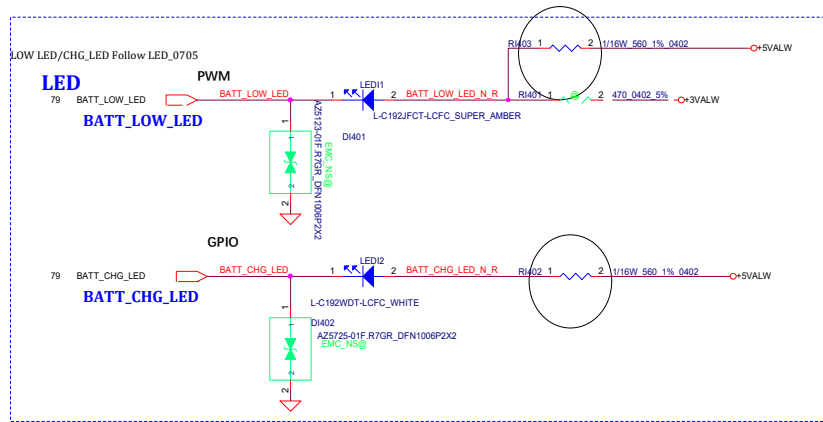
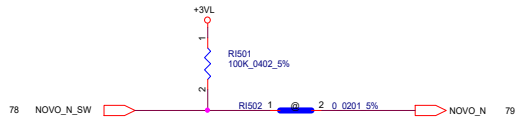


GPIO_SCL_R Follow Intel_0707



LCFC
Rev 0.3
Sheet 79 of 110

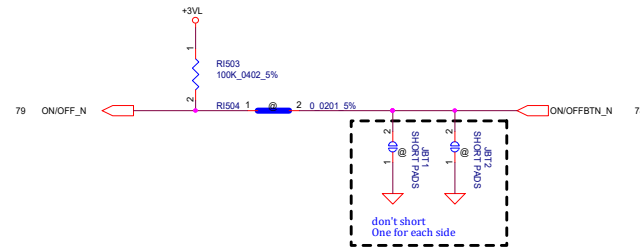
NOVO BUTTON




Power LED
check S750_ARH IO Board_0705

PWR BUTTON

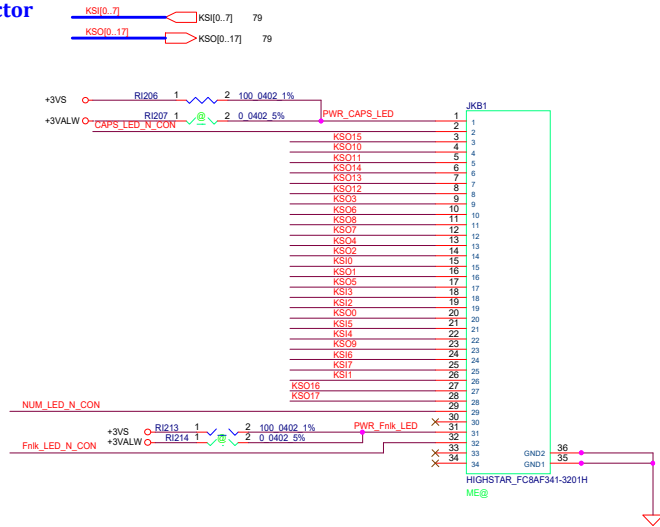
Nove button:follow S750 RI504 0R , Intel 2.2k



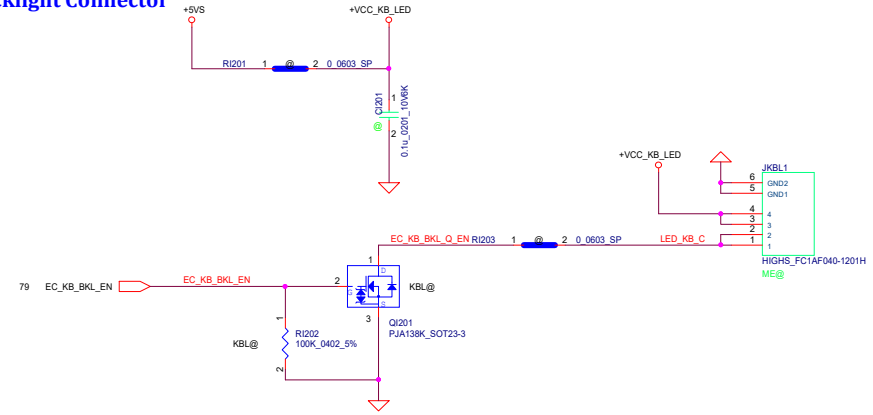
		Gradual 1s on, Gradual 1s off, 2s off	
LED	State	LED Behavior	
State (Same as the power button LED)	System on	White, on (battery: 21%-100%)	
		500ms on, 500ms off (battery: 0%-20%)	
	Standby LED closed		
	System off	OFF	
Charging	Battery only	OFF	
	Charging	Amber on (battery: 1%-90%)	
		White on (battery: 91%-100%)	

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Scale	Document Number	LED/Button			Rev 0.3
Date	Tuesday, December 21, 2021	Sheet	80	of	110

K/B Connector

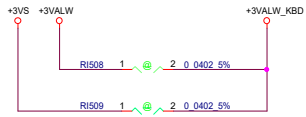


KB Backlight Connector

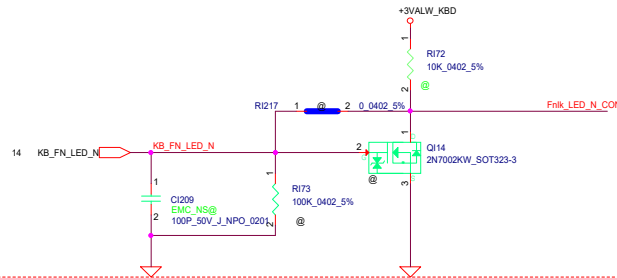


the diffrent with module:
1.module No 15 KB,S360&V14V15 have

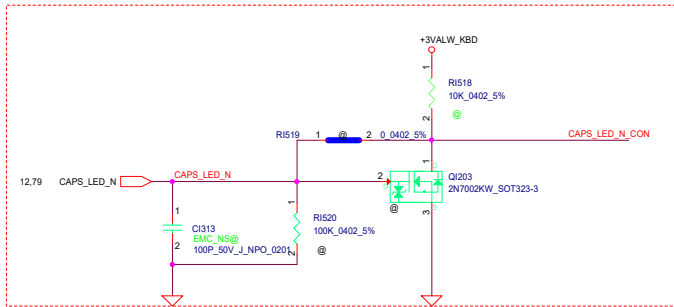
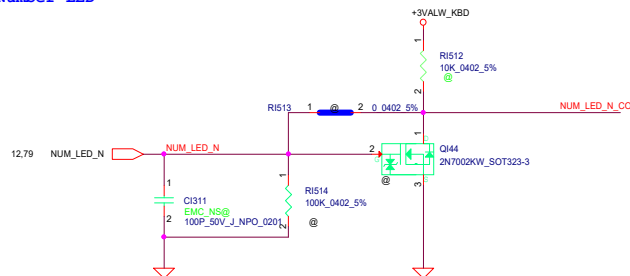
K/B Connector



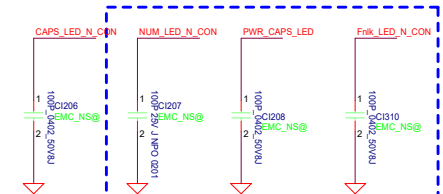
Flnk_LED#_Follow S550_are_0706



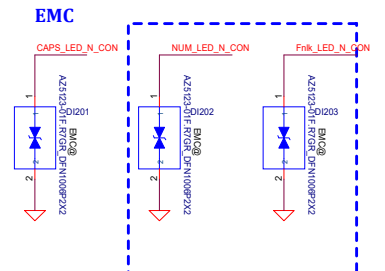
ADD Number LED




CI209/CI313/CI311 unstuff_SIT_1003



close to Conn



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Size	C	Document Number		KB/KBEL_CONN		Rev 0.3
Date:	Tuesday, December 21, 2021		Sheet	81	of	110

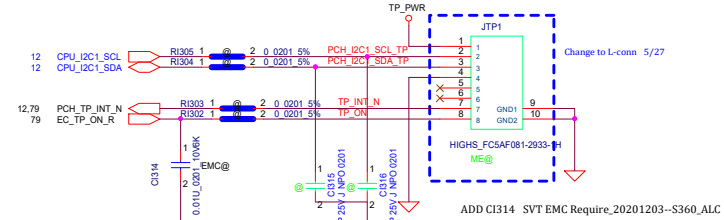
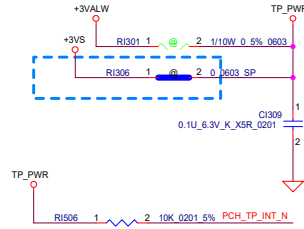


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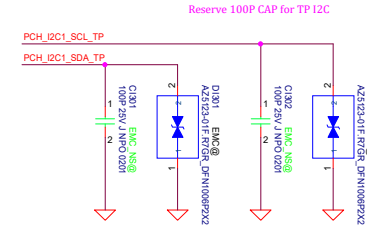
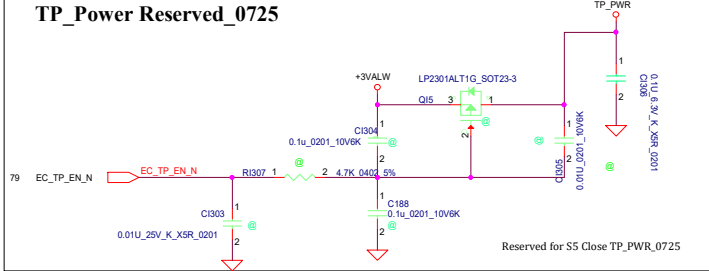
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Size	Document Number		
C	Anti Ghost KB	Rev	0.3
Date:	Tuesday, December 21, 2021	Sheet	82 of 110

Touch Pad (the diffrent with Base MODULE: 1.Module no RI306,S360&V14&V15 Rerserve) Intel 备注

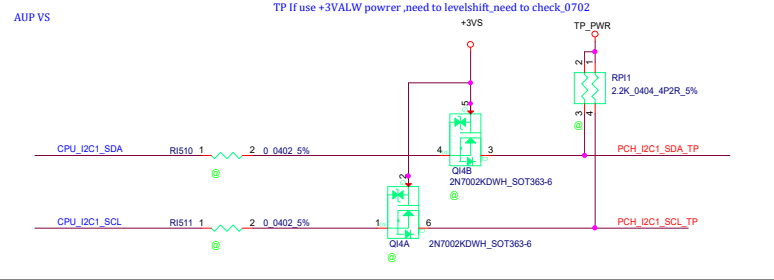
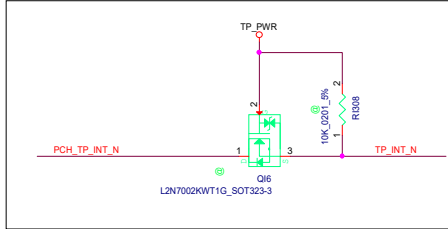
Need support wake up by touch pad
Follow latest UE spec



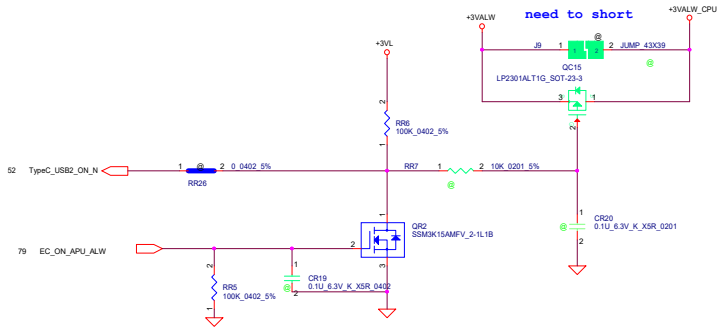
TP_Power Reserved_0725



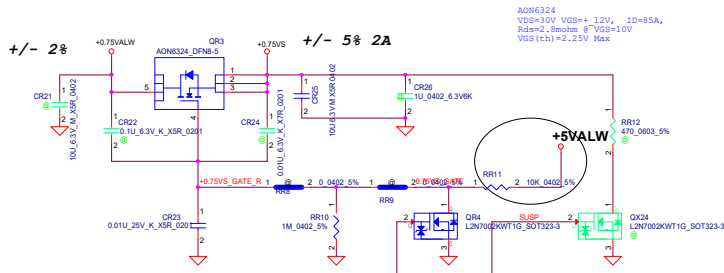
Follow S750_ARH ,S750_ARH APU USE S5 Power,SO Reserve Mosfet_0708



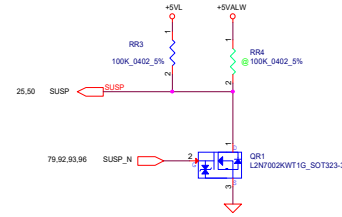
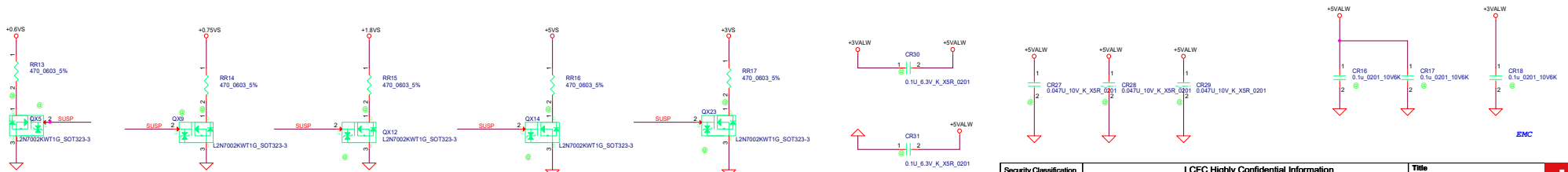
TO +3VALW_APU



TO +0.75VS



For DisCharge



Q1: change 2N7002 footprint SOT363-6 to sot323-3

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Size	Document Number		Rev		
Custom	DCDC SYSTEM PWR		0.3		
Date: Tuesday, December 21, 2021 Sheet 84 of 110					

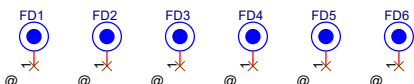


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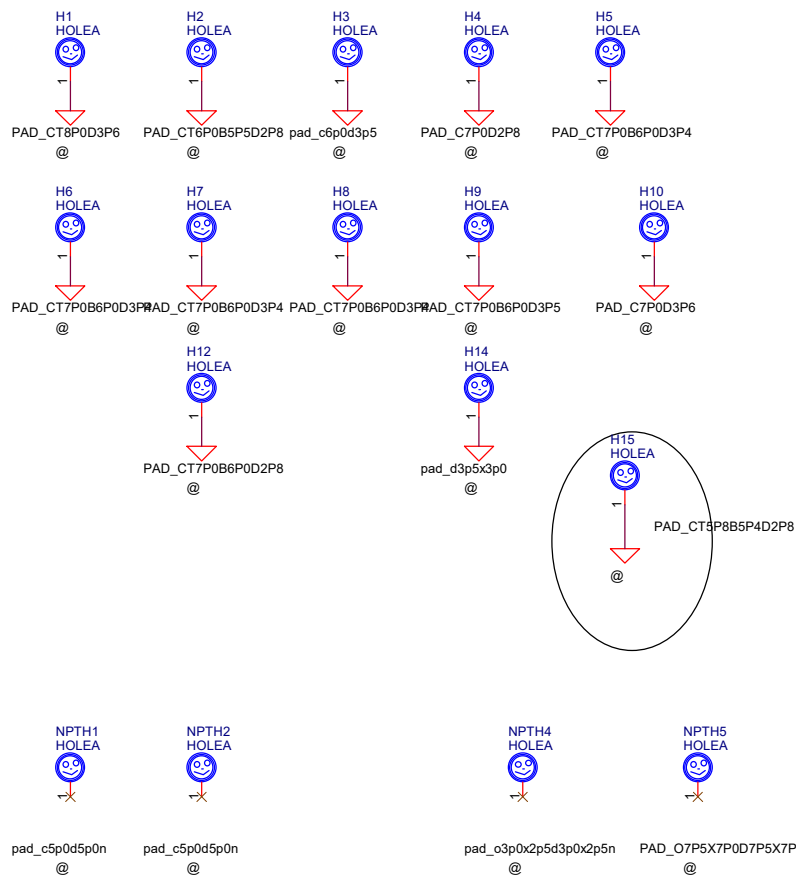
Title		LCFC	
Size	Document Number		Rev
C	DCDC MS PWR		0.3
Date:	Tuesday, December 21, 2021	Sheet 85 of 110	

Rev
0.3

PCB Fedical Mark PAD

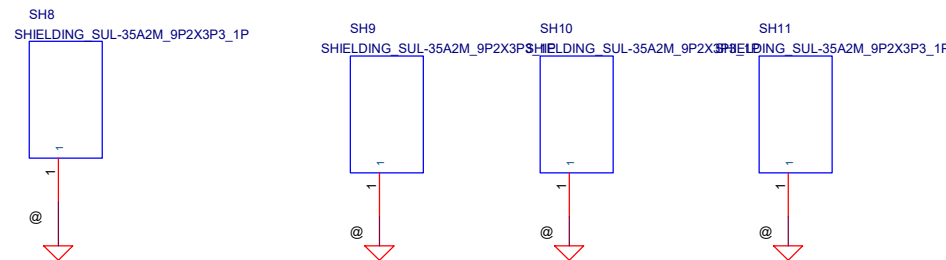


Hole



MD Shielding

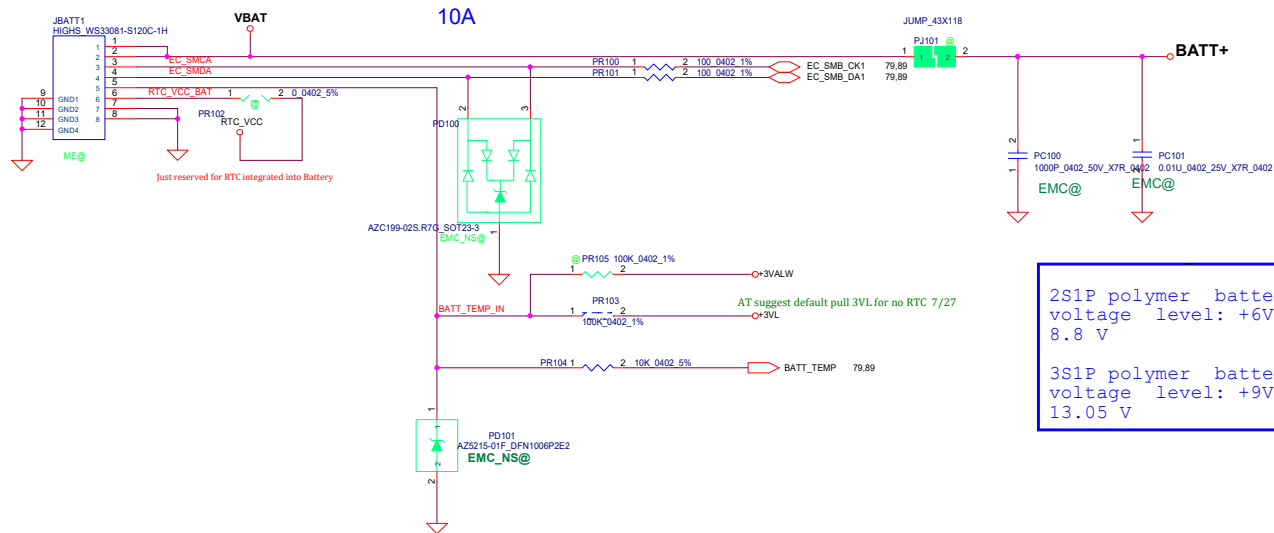
SO-DIMM Shielding



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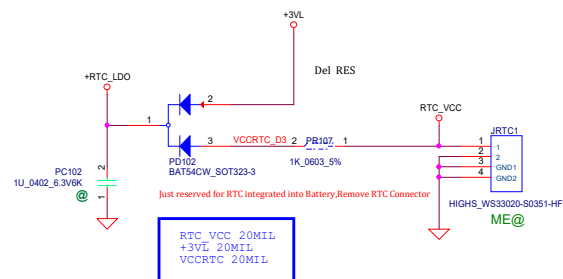
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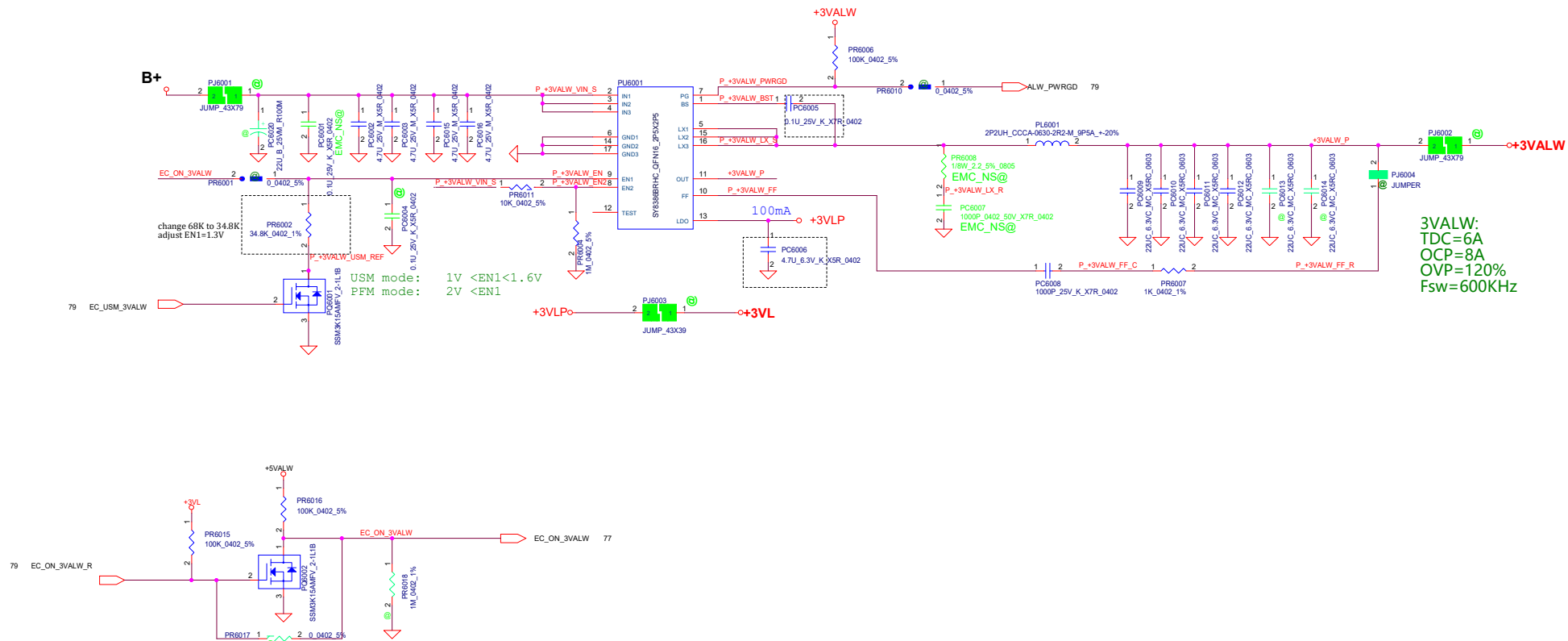
Hole/Shielding

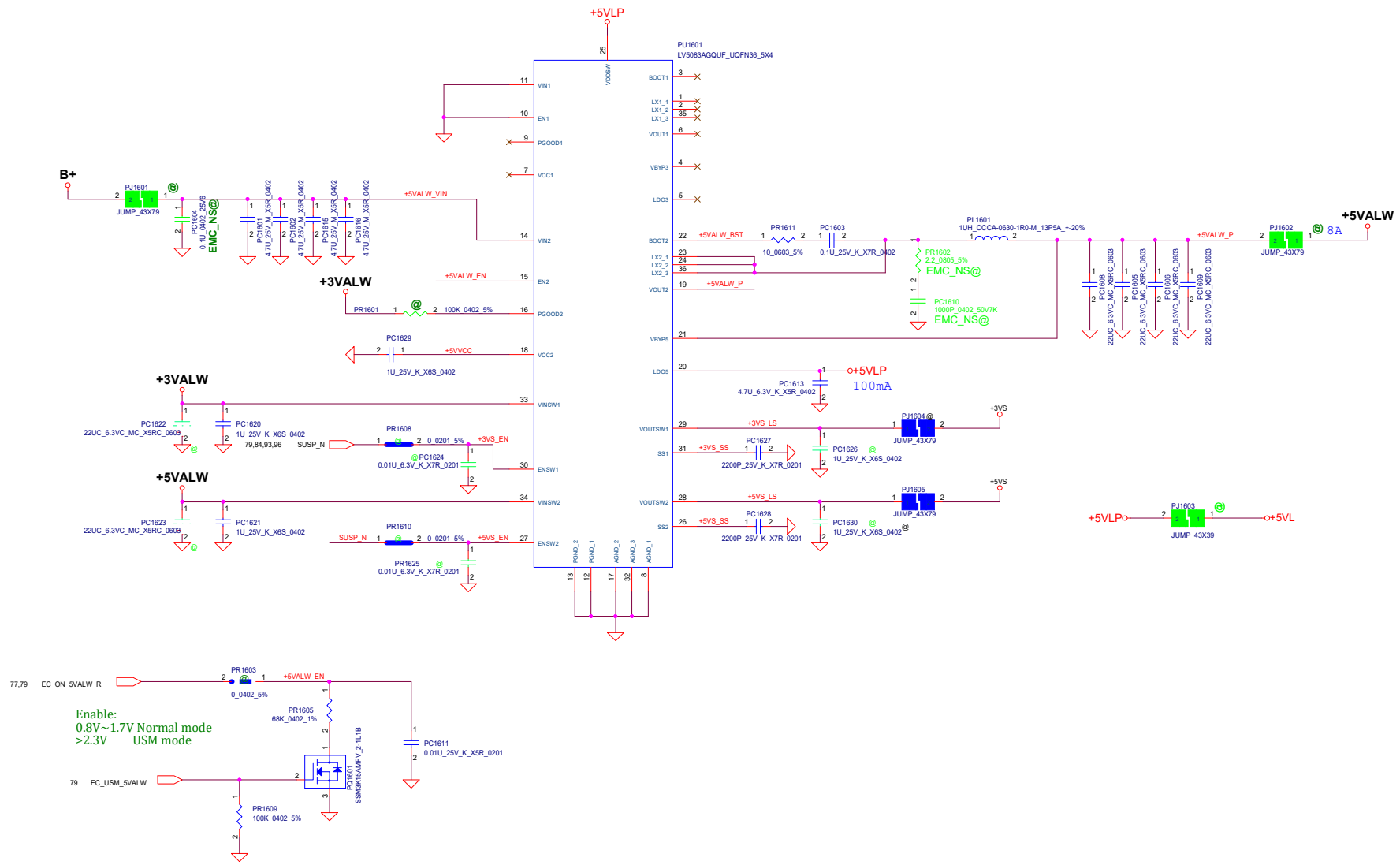


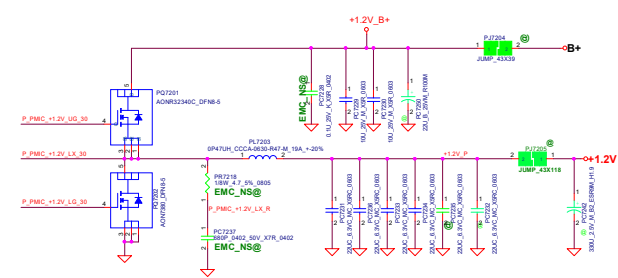
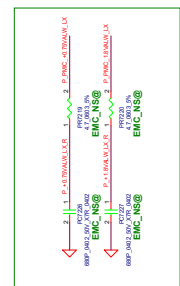
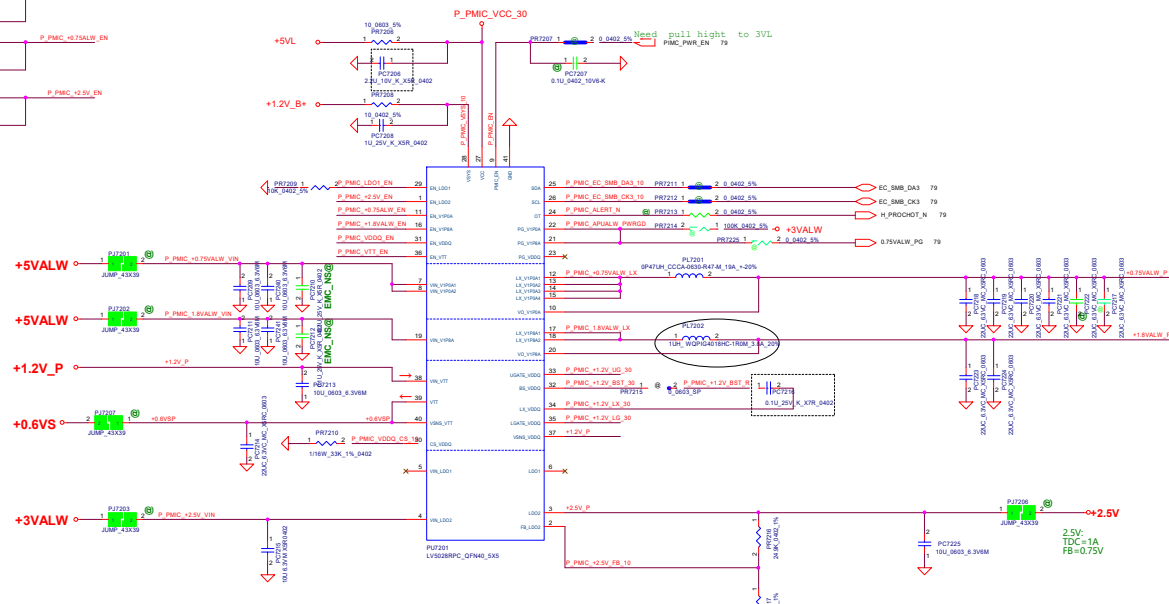
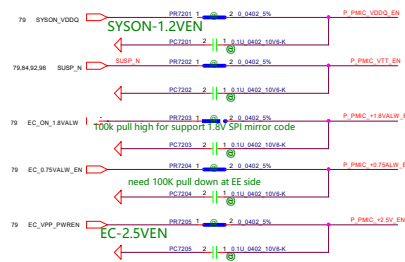
2S1P polymer battery
voltage level: +6V ~
8.8 V

3S1P polymer battery
voltage level: +9V ~
13.05 V

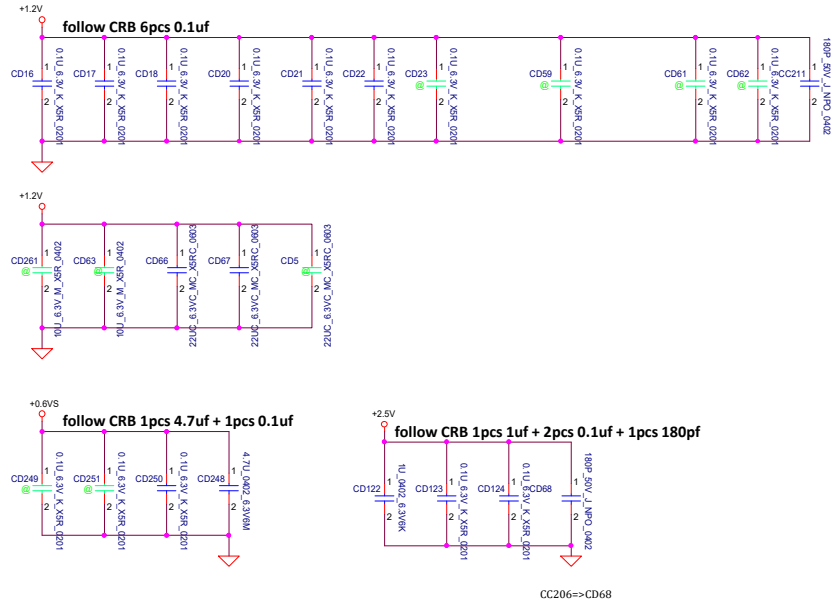




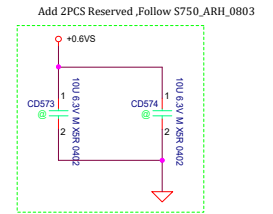
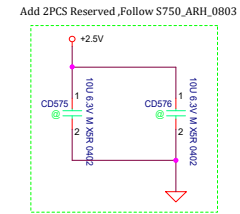
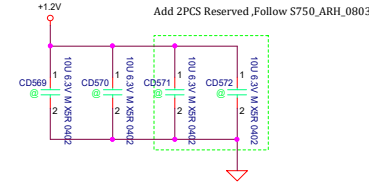




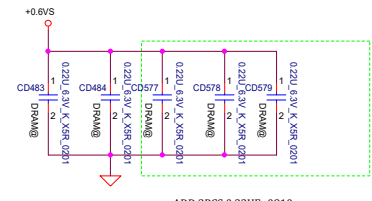
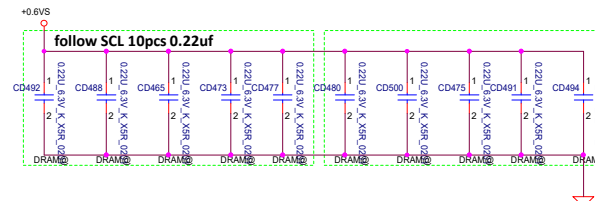
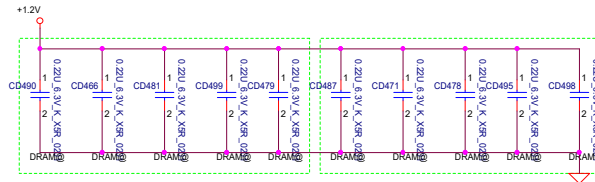
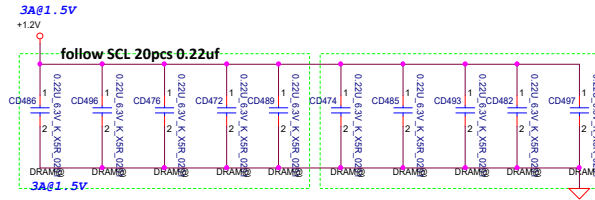
EE Side Channel A SODIMM
Follow S350_ARE_0803

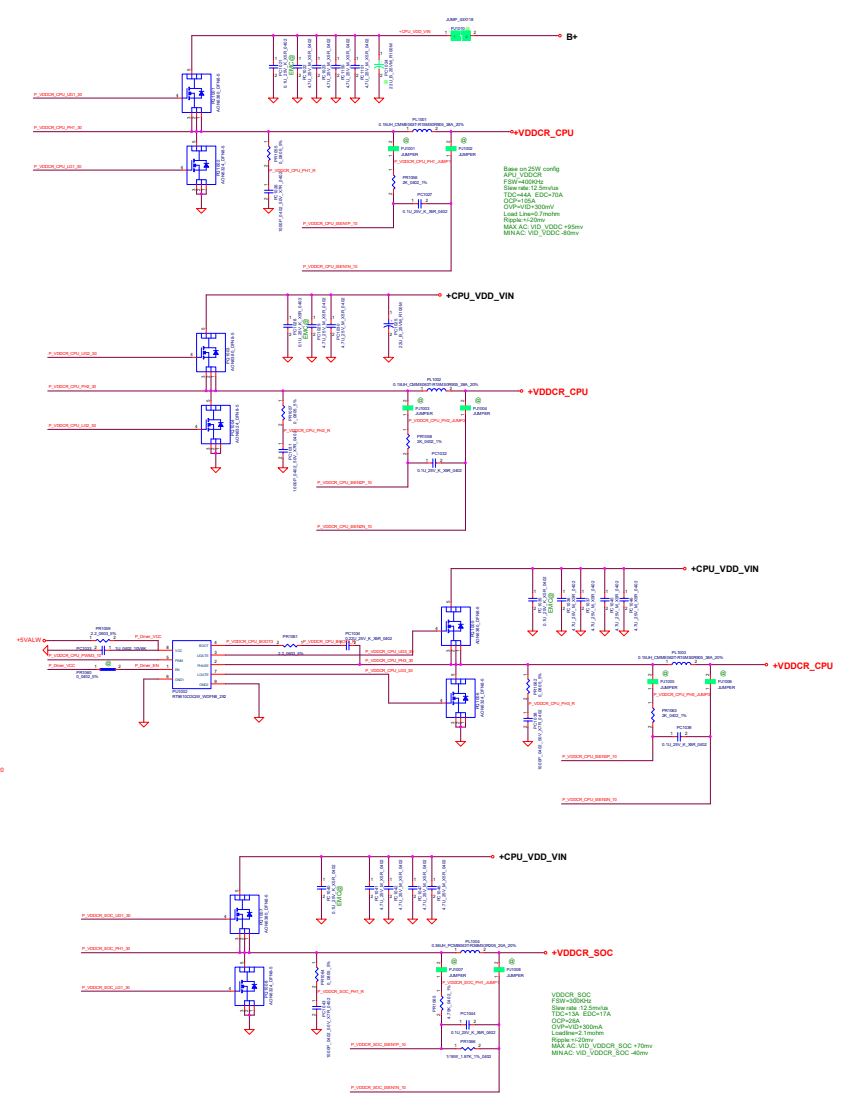


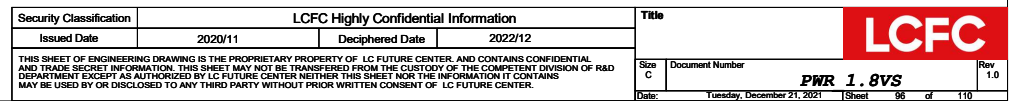
EE Side Channel B MD



Layout Note: Place near DRAM





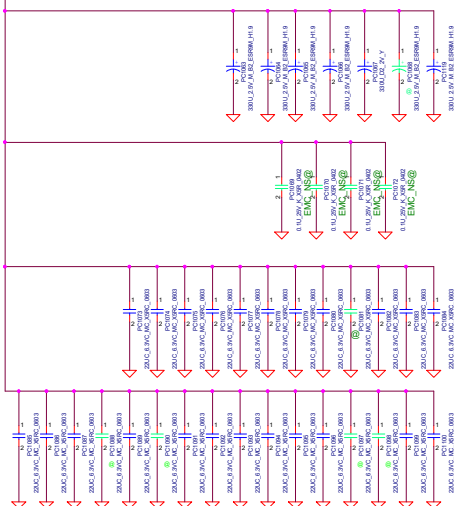




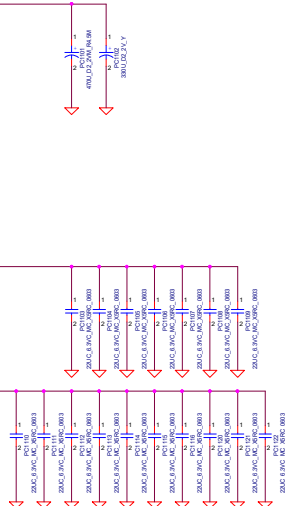
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+VDDCR_CPU



+VDDCR_SOC



5	4	3	2	1
D				
C				
B				
A				
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